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2021 JETTA-TTTC Best Paper Award

Thiago Copetti, Guilherme Cardoso Medeiros, Mottaqiallah Taouil, Said Hamdioui, Letícia Bolzani Poehls, and Tiago Balen, "Evaluation of Single Event Upset Susceptibility of FinFET-based SRAMs with Weak Resistive Defects," Journal of Electronic Testing: Theory and Applications, Volume 37, Number 3, pp. 383–394, June 2021

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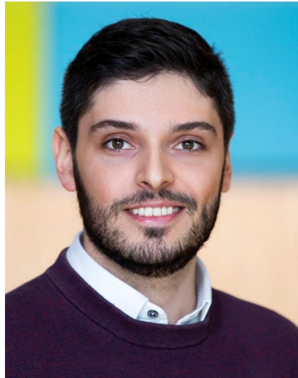
Abstract Fin Field-Effect Transistor (FinFET) technology enables the continuous downscaling of Integrated Circuits (ICs), using the Complementary Metal-Oxide Semiconductor (CMOS) technology in accordance with the More Moore domain. Despite demonstrating improvements on short channel effect and overcoming the growing leakage problem of planar CMOS technology, the continuity of feature size miniaturization tends to increase sensitivity to Single Event Upsets (SEUs) caused by ionizing particles, especially in blocks with higher transistor densities such as Static Random-Access Memories (SRAMs). Variation during the manufacturing process has introduced different types of defects that directly affect the SRAM's reliability, such as weak resistive defects. As some of these defects may cause dynamic faults, which require more than one consecutive operation to sensitize the fault at the logic level, traditional test approaches may fail to detect them, and test escapes may occur. These undetected faults, associated with weak resistive defects, may affect the FinFET-based SRAM reliability during its lifetime. In this context, this paper proposes to investigate the impact of ionizing particles on the reliability of FinFET-based SRAMs in the presence of weak resistive defects. Firstly, a TCAD model of a FinFET-based SRAM cell is proposed allowing the evaluation of the ionizing particle's impact. Then, SPICE simulations are performed considering the current pulse parameters obtained with TCAD. In this step, weak resistive defects are injected into the FinFET-based SRAM cell. Results show that weak defects can positively or negatively influence the cell reliability against SEUs caused by ionizing particles.

Thiago Santos Copetti graduated in 2012 and received his Master of Science Degree in 2015, both in Electrical Engineering at Pontifical Catholic University of Rio Grande do Sul (PUCRS), Brazil. In 2020 he did his thesis defence at the Federal University of Rio Grande do Sul (UFRGS). At the moment, he works as a Postdoc at the Chair of Integrated Digital Systems and Circuit Design (IDS) at RWTH University, Germany. His fields of interest include Fault Tolerant Integrated Circuits, Memory Testing, Single Event Upset (SEU) and Negative Bias Temperature Instability (NBTI) Aware, Design of Integrated Circuits and Memories, and also emerging technologies, such as memristors.



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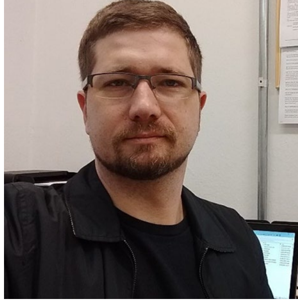

Tiago Roberto Balen received the Electrical Engineering degree, MSc and PhD degrees from Federal University of Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, in 2004, 2006, and 2010, respectively. His research interests include analog and mixed-signal test, built-in-self test, programmable analog devices, fault tolerant circuits and radiation effects on electronic systems. He has published more than 70 papers on these topics in conferences and journals, receiving four "Best Paper Awards". He has participated of the organizing committee of several conferences, such as LATS (steering committee member), LASCAS, IMSTW and SBCCI. He is an IEEE member with active participation in several societies and committees: TTTC, CEDA, CAS, EDS and SSCS. Currently, he is an associate professor at the Electrical Engineering department and head of the graduate program on Microelectronics (PGMICRO) of UFRGS.

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