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Comparison of the Output Parameters of the Memristor-based Op-amp Model and the Traditional Op-amp Model

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Abstract
A new operational amplifier (op-amp) model has been proposed using a memristor emulator based on the linear TiO_2 drift model. Simulation studies and numerical analyses of the new op-amp model designed using memristor are given. Frequency, unit, switching and electrical characteristic tests of the proposed op-amp model were performed. The parameter comparisons of the traditional op-amp and the proposed op-amp model are given in a detail table. In addition, the efficiency of the proposed op-amp model was realized with application circuits, and the reliability of the system was verified with the results.

Keywords Linear TiO_2 drift model · Memristor emulator · Operational amplifier · Op-Amp parameters

1 Introduction

Applications such as digital, analog and control systems are becoming increasingly important today due to their efficiency, scalability and reliability. Especially in such integrated application circuits, op-amp integrated models that act as amplifiers are critical. In the control applications of multi-input and multi-output systems, the basic element requirement that will enable the required impulse response to give the output response in a short time is created by op-amps [2, 8, 13, 23, 39, 45].

Parameters such as an op-amp's slew rate, common mode suppression ratio (CMRR), input and output offset currents and voltages, power consumptions, maximum signal processing speeds, switching parameters are critical in digital, analog and control applications [2, 6, 10, 12, 13, 17, 20, 23, 24, 35, 39, 42]. Undesirable increases in these parameters and high speed demands can cause voltage and current oscillations and even harmonics at the output. At this point, we come across the memristor, which is a semiconductor element. Due to its self-excited characteristics in a circuit, the memristor takes circuit theory one step further. The op-amp model designed using memristor proposes important solutions to the above-mentioned problems [19, 29, 30, 32, 34, 36, 37, 43, 46]. Especially when looking at the stages in the op-amp equivalent internal model, it was understood that the use of memristor in the level shift stage makes the signal transition between the input and output stages faster. Another advantage of the proposed op-amp model over traditional models was that it significantly increased the rate of slew parameter. At this stage, the op-amp layers on which the memristor can be placed were examined in detail. Element values that can work stably with the memristor in each layer were calculated. The advantages of the proposed op-amp model over the existing models were revealed. Finally, the accuracy and applicability of the proposed op-amp model has been extensively studied theoretically and supported by experimental and simulation results. In addition, some numerical analyses were carried out with the MATLAB program and contributed to the solutions.

2 Linear Dopant Drift $Ti0_2$ Memristor Emulator Circuit Model

Chua's first emulator circuit, which exhibited memristive behavior, consisted of many analog elements [7, 41]. Later, many emulator circuits began to be derived and implemented [22, 26–30]. In this study, the linear dopant drift TiO_2 memristor emulator circuit given

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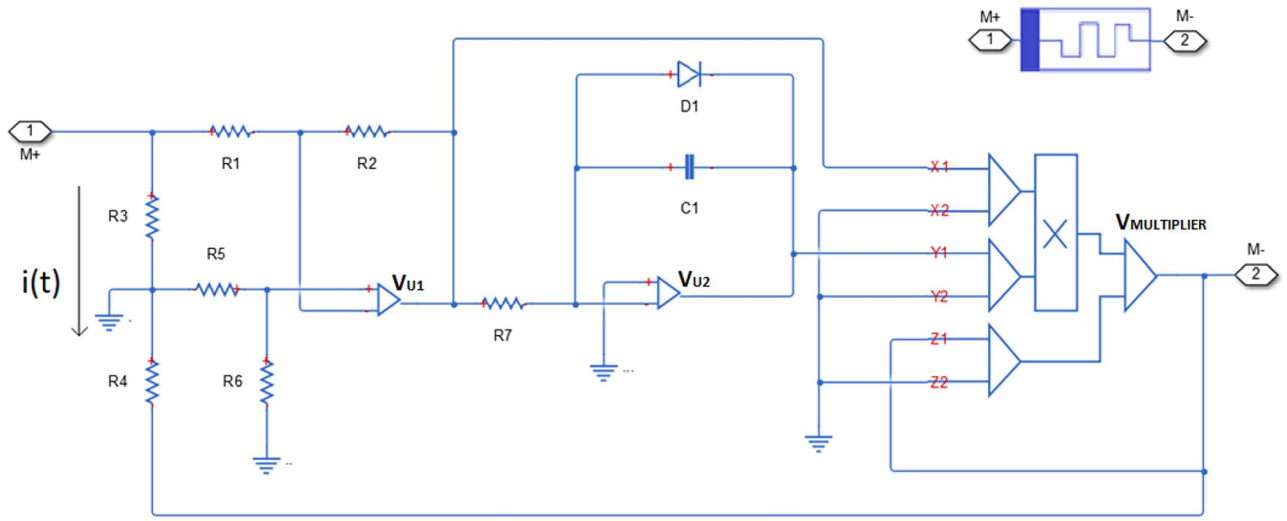


Fig. 1 Linear dopant drift $Ti0_2$ memristor emulator circuit diagram

in Fig. 1 was used. This circuit consists of a differential amplifier, an integrator circuit and an analog multiplier.

When an AC voltage is applied between the $M+$ and $M-$ points, the voltage expression on the R_3 resistor is expressed as in Eq. 1.

$$v_{R3} = i(t)R_3 \tag{1}$$

$v_{R3}(t) = v_{in}$ enters the differential amplifier circuit and creates the output voltage v_{U1}. The output voltage of the differential amplifier is shown in Eq. 2.

$$v_{U1} = v_{in}\frac{-R_2}{R_1} = i(t)\frac{-R_3R_2}{R_1} \tag{2}$$

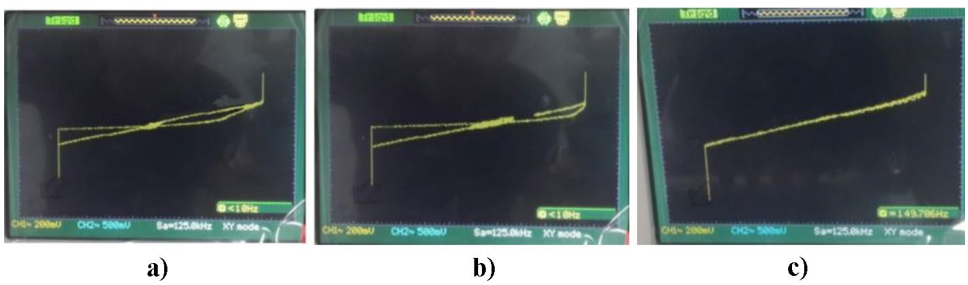
In this equation, the memristor load and current are multiplied by each other. It can be designed using the AD633, an analog multiplier whose voltage is proportional to the product of the memristor charge. The output of AD633 is $v_{MULTIPLIER} = v_{U1}.v_{U2}/10$ according to the statement given in the catalog. If it is applied to the circuit in Fig. 1, the output voltage of the analog multiplier is calculated as in Eq. 3.

$$v_{MULTIPLIER} = -\left(\frac{R_2R_3}{R_1}\right)^2\frac{1}{R_7C_1}q(t)i(t) \tag{3}$$

This voltage is non-linear due to the point product of the memristor load and the current. Another non-linearity of the memristor emulator, which does not appear in this equation, is due to the diode characteristic. The output voltage of the multiplier is added to the V_{R3} voltage as negative feedback. Thus, the expression for the memristor emulator input voltage or voltage at AB terminals is shown as in Eq. 4.

$$v_{AB} = v_{mem} = \left(R_3 - \left(\frac{R_2R_3}{R_1}\right)^2\frac{1}{R_7C_1}q(t)\right)i(t) \tag{4}$$

Figure 2 shows the hysteresis curve of the memristor emulator circuit at different frequencies. It has been stated that as the frequency is increased, the hysteresis curve gradually decreases and shows a memristive behavior. In addition, in many memristor emulator circuits, the behavior of the memristor can be changed by changing the values of especially capacitive values or other passive circuit elements [9, 16, 26,



a) **b)** **c)**

Fig. 2 Hysteresis curves of the memristor emulator fed with sinusoidal voltage at different frequencies; **a**) 8 Hz, **b**) 9 Hz and **c**) 150 Hz

29, 31, 33, 40, 44]. This flexibility shows us that the memristor has a working area not only at low frequencies but also at higher frequencies.

3 Proposed Op-Amp Model

In Fig. 3, the op-amp circuit designed using the memristor created in the PSpice program is shown. The memristor emulator is integrated with the op-amp as a subsystem. The effects of the memristor emulator placed in the op-amp internal circuit on the op-amp's output responses and specification tests are discussed in this section.

In general, the internal model of an op-amp consists of 5 basic stage as differential amplifier, bias current mirror, gain, level shift and output stage. The responses of the memristor emulator to be placed in the op-amp internal circuit were examined one by one at the specified stages and it was determined that the stage placement that would give the most optimum output response could be placed instead of the R5 resistor of the level change stage. Each stage of this proposed op-amp model is discussed in detail in the subsections [1, 3, 5, 8].

3.1 Difference Amplifier Stage

The input stage consists of a cascaded differential amplifier and a current mirror active load. This creates a transconductance amplifier that converts a differential voltage signal at bases $Q1$ and $Q2$ to a current signal at base $Q15$.

A voltage difference Vin at the op-amp inputs (pins 2 and 3) causes a small differential current $i_{in} \approx V_{in}/\left(2h_{ie}h_{fe}\right)$ in the bases $Q1$ and $Q2$. This differential base current causes a change in differential collector current in each leg by $i_{in}h_{fe}$. When $Q1$ is entered into the transconductance of $g_m = h_{fe}/h_{ie}$, if the current at the base of $Q15$ is regulated by Eq. 5;

$$\begin{aligned} V_{in} &= V^+ - V^- \\ i_{in} &\approx \frac{V_{in}}{2h_{ie}h_{fe}} \approx I_{C11} \\ I_{B15} &= \frac{V_{in}g_m}{2} \end{aligned} \tag{5}$$

This current takes $Q7$ further to conduction, which turns on the current mirror $Q5/Q6$. Thus, an increase in emitter current $Q3$ is reflected in an increase in collector current $Q6$. Increasing collector currents shunts more from the collector node and cause a decrease in base drive current for $Q15$ [2, 5, 11, 13, 23].

3.2 Gain Stage

The voltage gain stage (class A amplifier) consists of two NPN transistors $Q15/Q19$ connected in a darlington configuration and uses the output side of the current mirror $Q12/Q13$ as the collector load to achieve high voltage gain.

A current signal of I_{B15} at the base of $Q15$ causes a current of order $I_{B15}\beta^2 \approx I_{C19}$ in $Q19$. This current signal creates a voltage at the bases $Q14/Q20$ of the output transistors

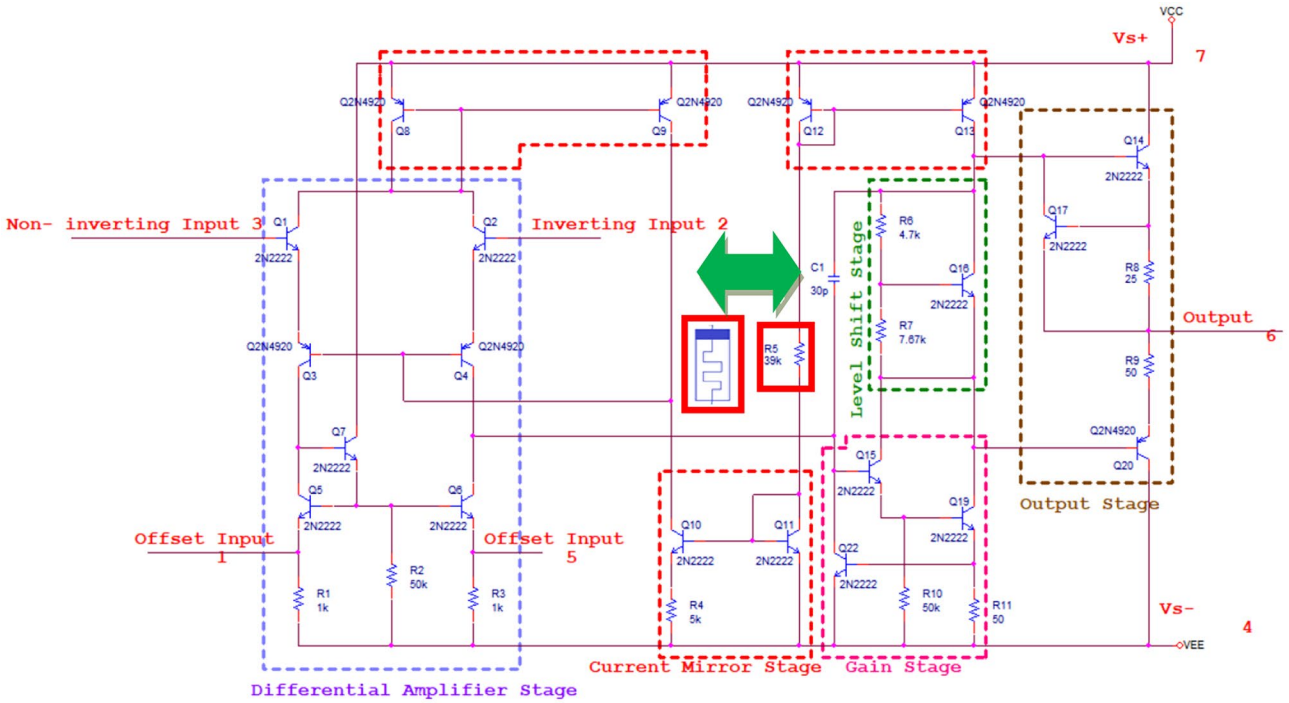


Fig. 3 Op-amp circuit designed using memristor

proportional to the h_{ie} of the respective transistor. If we rearrange Eq. 5 according to the emitter and collector currents of transistor $Q19$, Eq. 6 is obtained. [2, 5, 11, 13, 23].

$$I_{E19} \approx I_{C19} \approx \underbrace{\frac{V_{in}gm}{2}\beta^2}_{I_{B15}} \tag{6}$$

3.3 Current Mirror Stage

It determines $Q11$ and $Q12$ and the supplied supply voltage (resistor connecting$V_{S+} - V_{S-}$, $(39K\Omega)$), the current in current mirrors (matched pairs) $Q10/Q11$ and$Q12/Q13$. The collector current of $Q11$ is found as in Eq. 7.

$$I_{C11}x39K = V_{S+} - V_{S-} - 2V_{BE}, V_S = \pm 20V \tag{7}$$

The constant current in $Q11/Q12$ (as well as $Q13$) will be $\approx 1mA$. For a typical 741 of about $2mA$, a supply current dominates the quiescent supply current of these two bias currents [2, 5, 11, 13, 23]. In this circuit, if the collector current of $Q11$, which is obtained by placing a memristor imitation circuit instead of $39K\Omega$, is rearranged using Eq. 4, and then Eq. 8 is obtained.

$$I_{C11}xM(q) = V_{mem} = V_{S+} - V_{S-} - 2V_{BE}, V_S = \pm 20V$$
$$I_{C11} = \frac{\mathrm{v_{mem}}}{\left(R_3 - \left(\frac{R_2R_3}{R_1}\right)^2 \frac{1}{R_7C_1}q(t)\right)} \quad i_{mem} \approx I_{C11} \tag{8}$$

3.4 Level Shift Stage

In the circuit containing $Q16$, if $V_{BE16} \approx V_{R7.5K} \approx 0.7\mathrm{V}$ is accepted and voltage divider rule is applied to the base of the $Q16$ transistor, the collector–base voltages of the $Q16$ transistor are expressed as in Eq. 9.

$$V_{CB16} \approx 0.45\mathrm{V} \Rightarrow V_{CE16} \approx \left|V_{BE14} - V_{BE20}\right| \approx 1.0\mathrm{V} \tag{9}$$

From the current differences in the voltage divider resistors of the $Q16$ transistor, the current value in the base can be obtained as in Eq. 10.

$$I_{R4.5K} - I_{R7.5K} \approx \mathrm{I_{B16}} \tag{10}$$

Then the output voltage expression can be derived as in Eq. 11.

$$\begin{aligned} Vout &= \left|V_{BE14} - V_{BE20}\right| + \mathrm{R_{50\Omega}I_{E20}} - \mathrm{R_{25\Omega}}\left(\beta \mathrm{I_{B14}} - \mathrm{I_{B17}}\right) \\ Vout &= \left|V_{BE14} - V_{BE20}\right| + \mathrm{R_{50\Omega}I_{E20}} - \mathrm{R_{25\Omega}}\left(\beta\left(\mathrm{I_{C11}} - \mathrm{I_{B16}} - \mathrm{I_{C17}}\right) - \mathrm{I_{B17}}\right) \end{aligned} \tag{11}$$

Equation 12 can be obtained by placing the memristor current and voltage expressions into Eq. 11 by making use of the Eq. 8 expression.

$$Vout = \left|V_{BE14} - V_{BE20}\right| + \mathrm{R_{50\Omega}I_{E20}} - \mathrm{R_{25\Omega}}\left(\beta\left(\frac{\mathrm{v_{mem}}}{\left(R_3 - \left(\frac{R_2R_3}{R_1}\right)^2 \frac{1}{R_7C_1}q(t)\right)} - \mathrm{I_{B16}} - \mathrm{I_{C17}}\right) - \mathrm{I_{B17}}\right) \tag{12}$$

3.5 Output Stage

The output stage is Class AB complementary symmetry amplifier. It provides an output with an impedance of $\approx 50\Omega$ with current gain. Transistor $Q16$ provides the quiescent current for the output transistors and $Q17$ limits the output current.

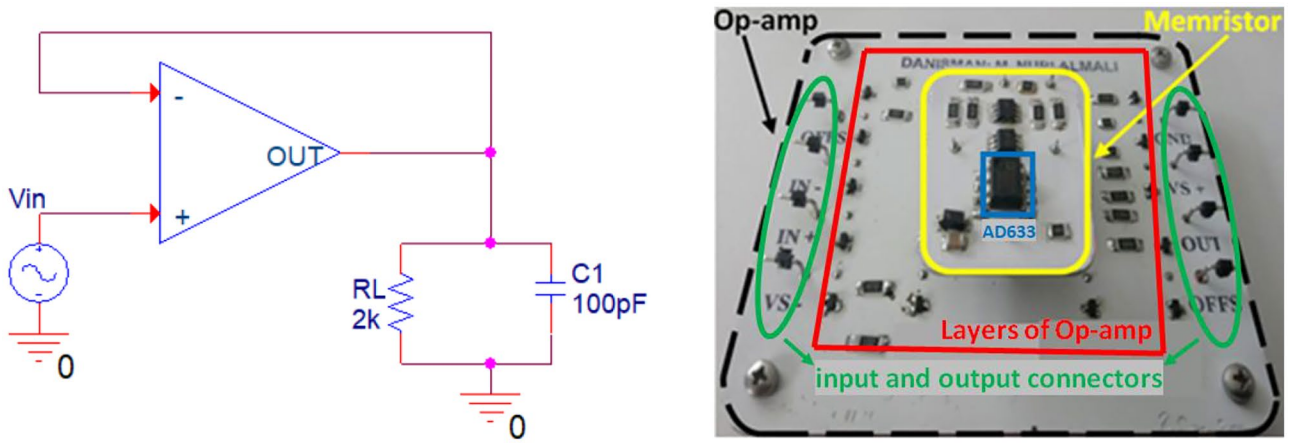


Fig. 4 Slew rate test circuit simulation and experimental setup of op-amp designed using memristor

4 Experimental Setup

In Fig. 4, the memristor emulator application circuit has been made into an integrated and ergonomic structure with surface mountable devices (SMD). Then, it was combined with op-amp layers for use in analog studies. One of the biggest challenges of the op-amp designed using memristor was the choice of transistor. When choosing both NPN and PNP transistors, attention was paid to ensure that the same catalog values of the same company were identical. Based on beta values, current–voltage characteristics, operating temperature range and the most stable output response in the pre-application circuits, BC237 transistor was preferred for NPN and BC307 transistor was preferred for the identical PNP. The circuits in Figs. 1 and 3 were combined into a single structure. Appropriate element values were selected according to the analog application desired to work with. Some of the crucial points in the experimental setup are as follows: using an electrolyte capacitor in the memristor emulator and choosing approximately 100nF allows you to work in a wider frequency range. There are different analog multipliers in the market. In the literature, the use of analog multiplier chip AD633 is generally preferred in the memristor emulators for stable outputs especially for application circuits. Non-static protective paint was used on the experimental setup to minimize the capacitive effects that may occur due to the Miller Effect during the high frequency tests. Making the

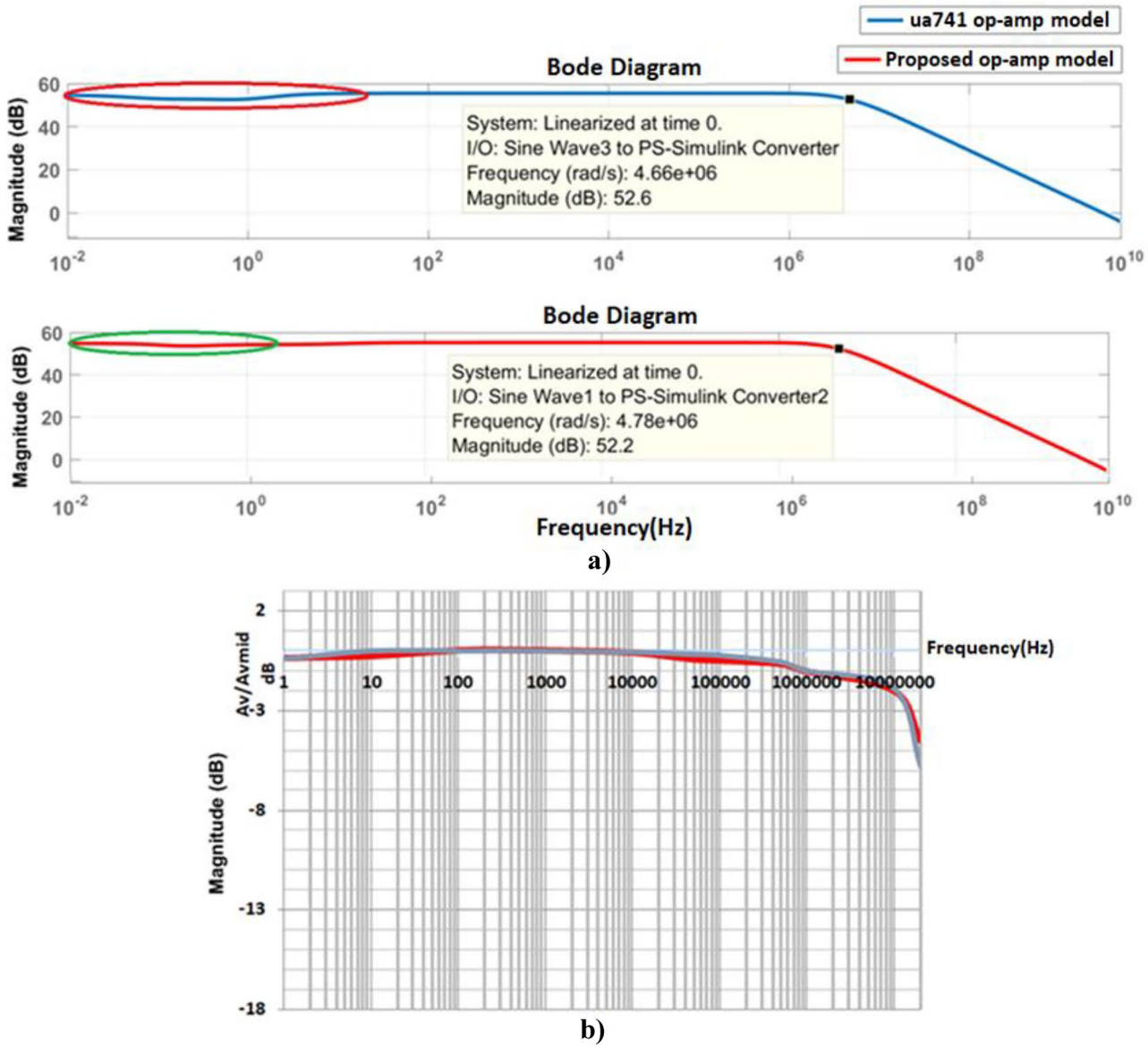


Fig. 5 Bode diagrams of op-amp designed using memristor and traditional op-amp model; **a**) simulation results and **b**) experimental result

proposed op-amp model with 8 connectors (green region) makes it more widely used. The red region shows the inner layers of the op-amp circuit. The memristor emulator (yellow region) was placed in the middle to provide an ergonomic structure with the op-amp.

4.1 Op-Amp Specification Parameters

In order to reveal the general behavior of an op-amp, its response on the specification parameters must be known [2, 6, 13, 17, 20, 23, 35, 39, 42]. In this section, both simulation and application tests of the parameters specified in this section were performed. These tests were carried out under nominal test conditions, that is, at ideal temperature and pressure.

Before the op-amp specification parameter tests given above were performed on the test circuit given in Fig. 4, the proposed op-amp model was subjected to the slew rate test. This test was accepted as a prerequisite for the specified parameters and the predictability of the desired results was discussed.

In Fig. 5, the op-amp's gain bandwidth, maximum signal frequency and slew rate tests were performed at different voltages and frequencies [4, 13, 14, 21, 23, 25]. These tests were carried out under nominal conditions by creating a simulation environment where the environment temperature, pressure and other physical conditions are the most ideal.

The maximum signal frequency at which an op-amp can operate depends on both its bandwidth (BW) and the slew rate of signal [14, 15, 18, 25, 38, 47]. In the simulation and experimental tests performed in Fig. 6, a sinusoidal signal such as $V_o = Ksin(2\pi ft)$ was used. The K and f values for this signal were gradually increased until the output signal of the op-amp crossovered. Then input signals from 1 mV to 10 V and from 10 Hz to 20 MHz and 100 MHz were given to traditional op-amp and proposed op-amp models.

When the simulation and application studies of different op-amp models were examined in the light of the predicted parameters [4, 13–15, 17, 21, 23, 25], it was observed that the proposed op-amp improved the regions where the traditional op-amp crossovered at high frequency and low voltages. The results obtained are comprehensively given in Table 1.

In another test parameter [13, 20, 23, 32] the operating point was determined by increasing the proposed op-amp input differential voltages under nominal conditions. Then, by giving dual (symmetrical) supply voltages, the output responses were examined under these conditions. When the catalogs of the manufacturers are examined, it is seen that the maximum rated tests of the op-amps are performed at $\pm 18V$ source voltage and $\pm 15V$ differential input voltage. These conditions were created for different op-amp models in the simulation environment. In the simulation environment, the source voltages were increased up to $\pm 22V$. The optimum power points are shown in Fig. 7 by connecting active and reactive loads on the test circuit.

When the simulation and experimental studies of different op-amp models were examined in the light of the predicted parameters, it was seen that the proposed op-amp had less power consumption compared to the traditional op-amp,

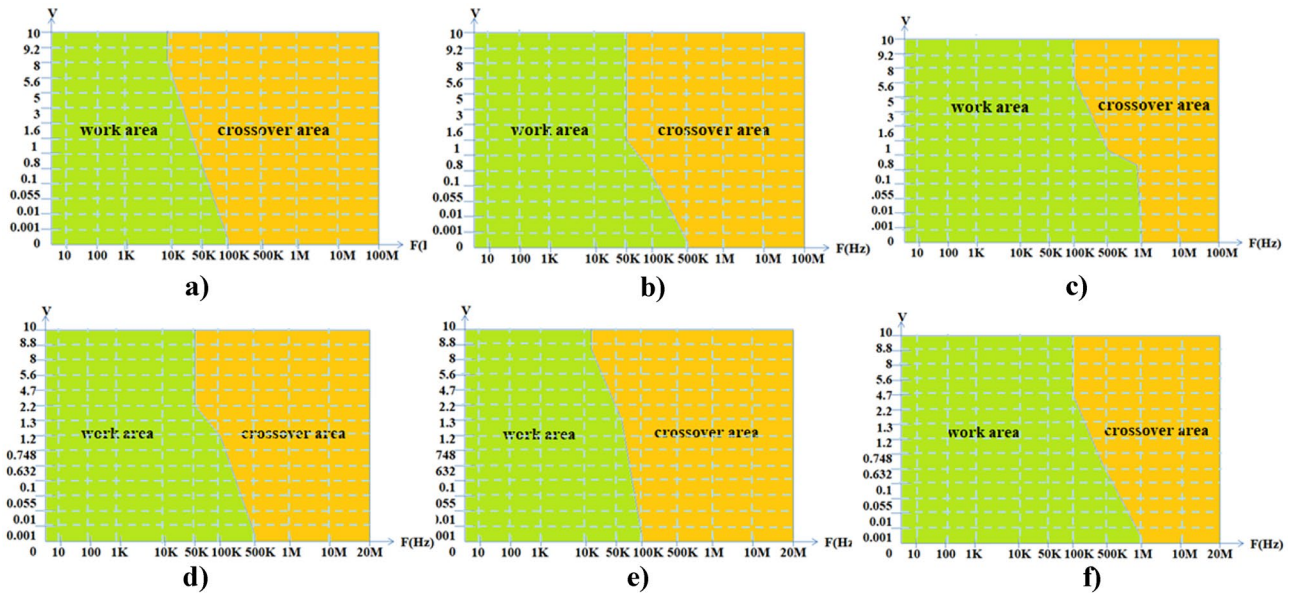


Fig. 6 The op-amp designed using a memristor and the slew rate operating regions of the traditional op-amp model; **a**) μa741 op-amp chip (approximate model), **b**) μa741 op-amp chip simulation, **c**) proposed op-amp simulation, **d**) μa741 op-amp chip (physical model), **e**) μa741 op-amp chip experimental and **f**) proposed op-amp experimental

Table 1 Frequency characteristic analysis of the proposed op-amp and $\mu a741$ op-amp

Frequency characteristic	Proposed op-amp		$\mu a741$ op-amp	
Parameter	**Simulation**	**Experimental**	**Simulation**	**Experimental**
Gain bandwidth	$4.78MHz$	$4.06MHz$	$4.66MHz$	$3.76MHz$
Maximum signal frequency	$500KHz/1V$	$500KHz/0.632V$	$50KHz/1.6V$	$100KHz/1.2V$
Slew Rate (SR)	$3.1V/\mu s$	$2.95V/\mu s$	$0.51V/\mu s$	$0.7V/\mu s$

especially considering the experimental results. The results obtained are comprehensively given in Table 2.

In this part, the output switching responses of different op-amp models under the same input voltages and under the same physical conditions; the rise and fall times were measured. First of all, a square signal was given to the input at a certain frequency and input voltage, and cut-off and turn-on conditions of the op-amps were examined. In Fig. 8, the times defined between 10 and 90% of the peak value of the input and output signals in both the rise and fall times [5, 13, 23] were determined by measuring.

When the simulation and experimental studies of different op-amp models were examined in the light of the predicted parameters [13, 20, 23], it was observed that the proposed op-amp improved the regions where the traditional op-amp crossovered at high frequency and low voltages. The results obtained are comprehensively given in Table 3.

Input voltage imbalances occurring at the input of the op-amp can cause the voltage occurring at the output of the op-amp to change. Input unbalance voltage; it depends on temperature, open loop gain and unbalance voltage. If the relationship between output voltage (V_O) and offset voltage (V_{IO}) according to the circuit in Fig. 9 is calculated according to Eq. 13;

$$V_O = AV_i = A\left(V_{IO} - V_{IO}\frac{R_{in}}{R_{in}+R_f}\right) \tag{13}$$

If the equation is solved for the V_O offset voltage, the voltages for each op-amp are calculated as follows.

$$21x10^{-3}V \approx V_{IO}\frac{20k\Omega + 1k\Omega}{1k\Omega} \rightarrow V_{IO(ua741\ op-amp\ simulation)} \approx 1mV$$

$$2.1x10^{-3}V \approx V_{IO}\frac{20k\Omega + 1k\Omega}{1k\Omega} \rightarrow V_{IO(proposed\ op-amp\ simulation)} \approx 100\mu V$$

$$15x10^{-3}V \approx V_{IO}\frac{20k\Omega + 1k\Omega}{1k\Omega} \rightarrow V_{IO(ua741\ op-amp\ experimental)} \approx 714.28\mu V$$

$$13.82x10^{-3}V \approx V_{IO}\frac{20k\Omega + 1k\Omega}{1k\Omega} \rightarrow V_{IO(proposed\ op-amp\ experimental)} \approx 658.09\mu V$$

I_B is the input offset current flowing through the bases of the input transistors in bipolar circuits. The value of this current depends on the current of the input stage and the gains of the input transistors β_F. Its typical value is between $10nA$ and $500nA$ for most BJT operational amplifiers [13, 23, 39]. In NPN transistors, since the input current flows from the base to the emitter (into the operational amplifier), it is positive, and for PNP transistors it is negative. In Fig. 10, the input bias currents at the inverting and non-inverting inputs of the operational amplifier are shown.

When the output voltage of the op-amp is or is $Vo = 0V$, the difference of the absolute values of the I_{B+} and I_{B-} currents is called the input unbalance current and the I_{OS} current is defined as in Eq. 14.

$$I_{OS} = |I_{B+}| - |I_{B-}| \tag{14}$$

According to this;

$$I_{OS(ua741\ op-amp\ simulation)} = |\mathrm{I_{IB+}} - \mathrm{I_{IB-}}| = |80\mathrm{nA} - 60\mathrm{nA}| \approx 20nA$$

$$I_{OS(proposed\ op-amp\ simulation)} = |\mathrm{I_{IB+}} - \mathrm{I_{IB-}}| = |365\mathrm{nA} - 364\mathrm{nA}| \approx 1nA$$

$$I_{OS(ua741\ op-amp\ experimental)} = |\mathrm{I_{IB+}} - \mathrm{I_{IB-}}| = |5.88\mathrm{nA} - 10.94\mathrm{nA}| \approx 5.06nA$$

$$I_{OS(proposed\ op-amp\ experimental)} = |\mathrm{I_{IB+}} - \mathrm{I_{IB-}}| = |455.2\mathrm{nA} - 455.8\mathrm{nA}| \approx 0.6nA$$

In operational amplifiers, when the input signal is the same, the operational amplifier should not produce an output. However, in practice, a very small output signal is produced in response to the common signal. The difference mode signal gain of the operational amplifier is quite large compared to the common mode signal gain. In this case, the CMRR value, which is the ratio of the difference-mode voltage gain to the common-mode voltage gain, is an important parameter [13, 42]. Figure 11

Table 2 Unit characteristic analysis of the proposed op-amp and $\mu a741$ op-amp

Unit characteristic	Proposed op-amp		$\mu a741$ op-amp	
Parameter	**Simulation**	**Experimental**	**Simulation**	**Experimental**
Total power consumption-P_D	$112.5mW$	$118.1mW$	$112.5mW$	$125.2mW$

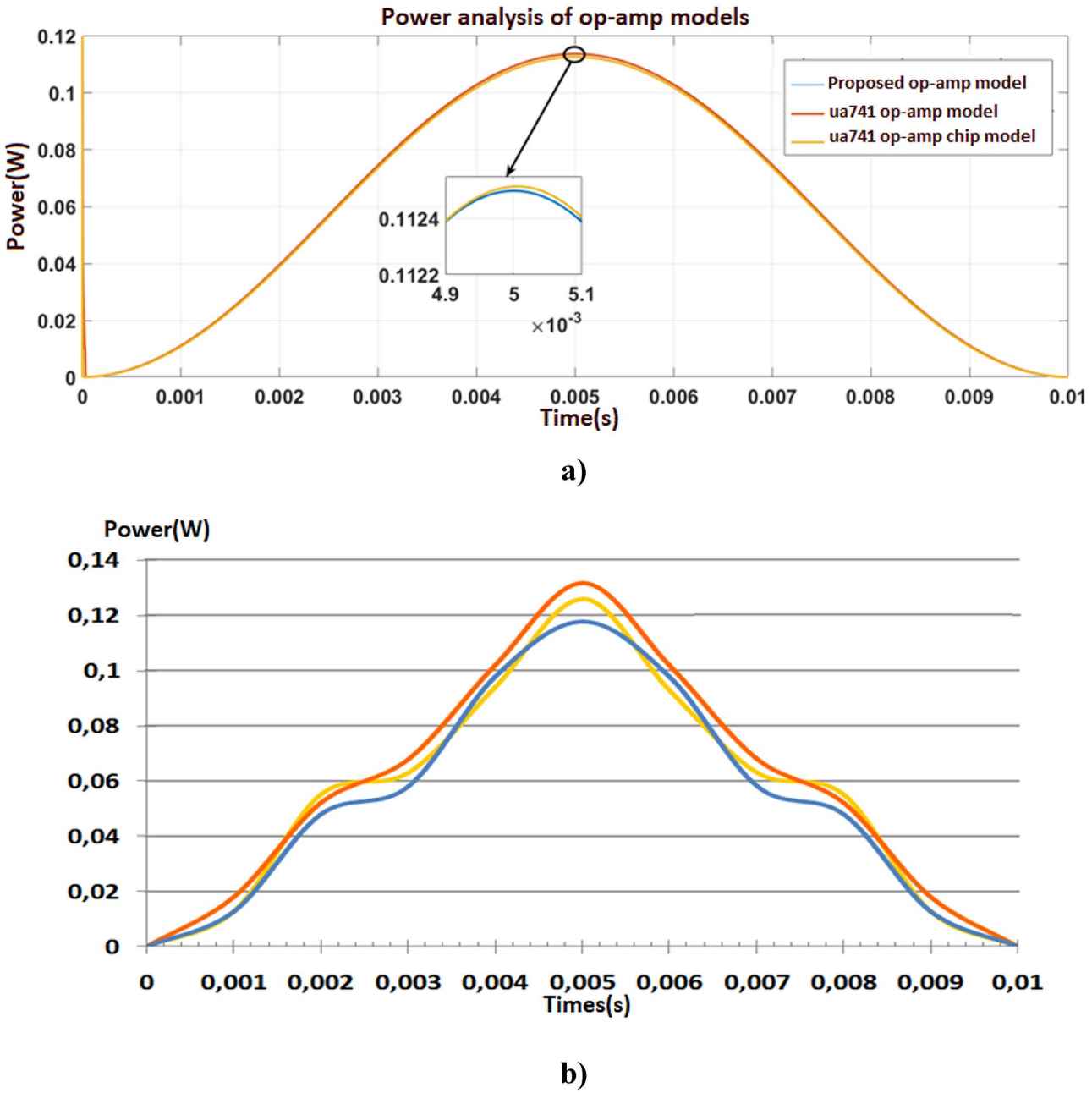


Fig. 7 Power consumption analysis of the proposed op-amp and traditional op-amp model; **a**) simulation result and **b**) experimental result

shows the schematic used to measure the conventional CMRR measurement test circuit value. If $R_2 \gg R_1$; CMRR;

$$CMRR = \frac{A_d}{A_c} = \frac{V_d}{V_c} \approx \frac{R_2}{R_1}\frac{V_s}{V_o} \tag{15}$$

$$CMRR_{(ua741\ op-amp\ simulation)} \approx 20log\left(\frac{100M\Omega}{1\Omega}\frac{1mV}{24.60}\right) \approx 72.18\boldsymbol{dB}$$

$$CMRR_{(proposed\ op-amp\ simulation)} \approx 20log\left(\frac{100M\Omega}{1\Omega}\frac{1mV}{13.61}\right) \approx 77.32\boldsymbol{dB}$$

$$CMRR_{(ua741\ op-amp\ experimental)} \approx 20log\left(\frac{100M\Omega}{1\Omega}\frac{1mV}{19.38}\right) \approx 74.25\boldsymbol{dB}$$

$$CMRR_{(proposed\ op-amp\ experimental)} \approx 20log\left(\frac{100M\Omega}{1\Omega}\frac{1mV}{15.23}\right) \approx 76.34\boldsymbol{dB}$$

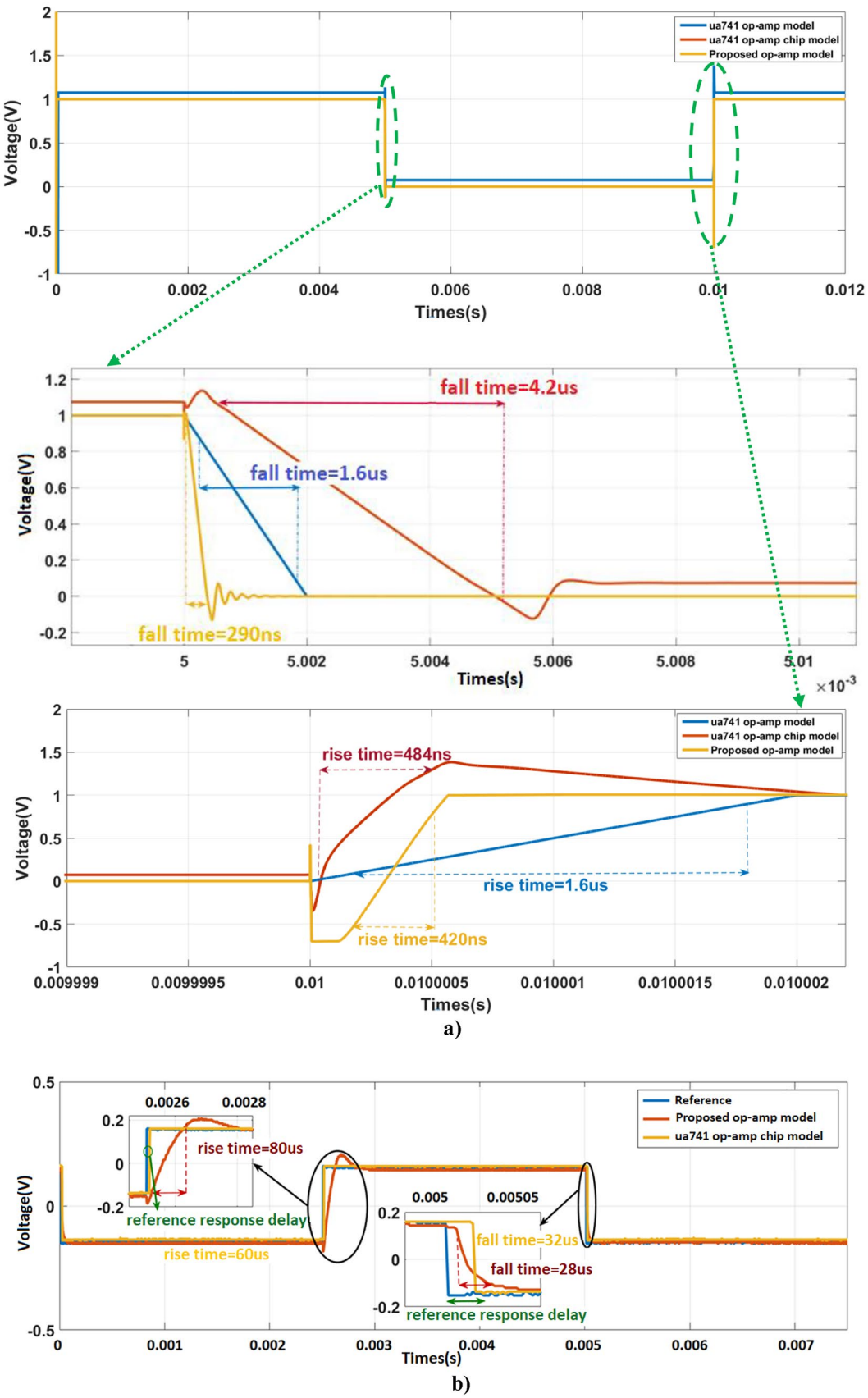


Fig. 8 The rise and fall times of the output signals of the traditional op-amp model with the proposed op-amp; **a**) simulation result and **b**) experimental result

Table 3 Switching characteristic analysis of proposed op-amp and $\mu a741$ op-amp

Switching characteristic	Proposed op-amp		μa741 op-amp	
Parameter	Simulation	Experimental	Simulation	Experimental
t_r Rise time	420ns	80us	1.6us	60us
t_d Fall time	290ns	28us	1.6us	32us

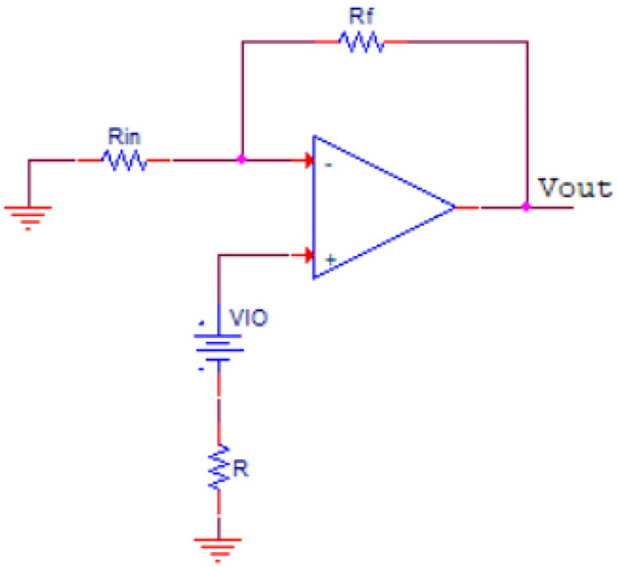


Fig. 9 V_{IO} offset voltage test circuit schematic

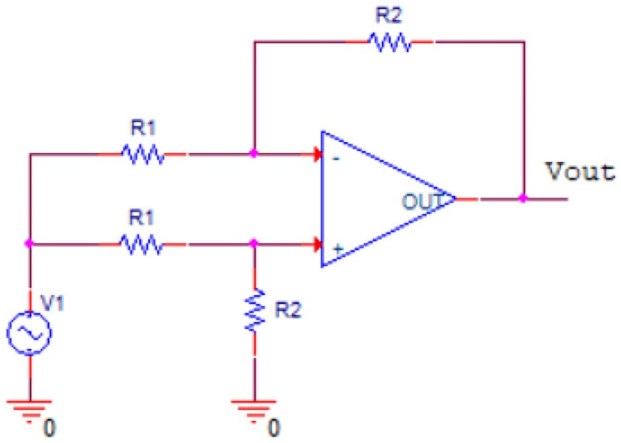


Fig. 11 CMRR measuring test circuit schematic

When the simulation and experimental studies of different op-amp models were examined in the light of the predicted parameters, it was seen that the proposed op-amp had significant improvements in the input offset voltage and current, as well as the CMRR value compared to the traditional op-amp. It has been observed that the input and output impedance values of the proposed op-amp model are higher than the traditional op-amp model. In particular, it is desirable that the input impedance be high. The results obtained are comprehensively given in Table 4.

Fig. 10 Input offset current test circuit schematic of inverting and non-inverting inputs

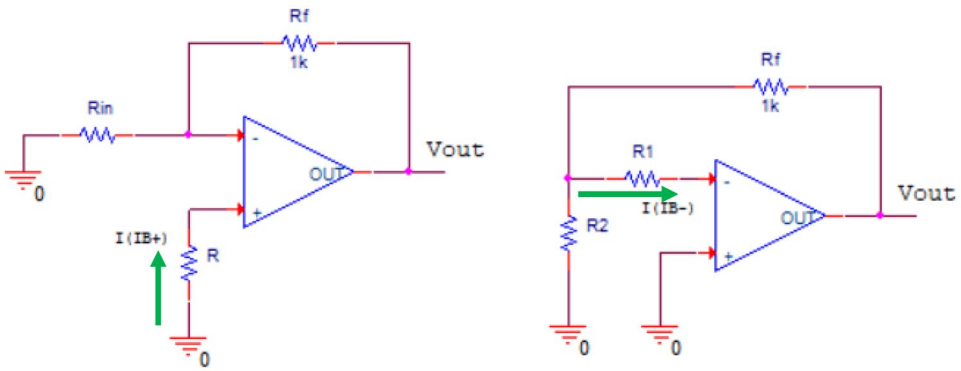


Table 4 Electrical characteristic analyses of the proposed op-amp and $\mu a741$ op-amp

Electrical Characteristic	Proposed op-amp		μa741 op-amp	
Parameter	**Simulation**	**Experimental**	**Simulation**	**Experimental**
V_{IO} Input offset voltage	$100\mu V$	$658.09\mu V$	$1mV$	$714.28\mu V$
I_{IO} Input offset current	1nA	$0.6nA$	20nA	$5.06nA$
$CMRR$ Common mode rejection ratio	$77.32dB$	$76.34dB$	$72.18dB$	$74.25dB$
r_i Input impedance	$2.77M\Omega$	$3.51M\Omega$	$2M\Omega$	$2.43M\Omega$
r_o Ouput impedance	755Ω	980Ω	110Ω	748Ω

5 Conclusion

In this study, a detailed comparison between the op-amp model designed using memristor and the traditional op-amp model is presented. When the input unbalance voltages and currents of the proposed op-amp are calculated respectively, it is seen that they are smaller than the traditional op-amp model. The small unbalance voltage and current increase the efficiency of the system. It was observed that the CMRR value was higher in the proposed op-amp model. If this value is high, it absorbs in the environment noise better and prevents it from being transferred to the output. It has been observed that the input and output impedance values are partially higher than the traditional op-amp in the proposed op-amp model. It was seen that these values were not an important criterion in the speed or performance of the op-amp, but made a difference in terms of low current. In future studies, in order to further reduce the output impedance value, the transistors used in the proposed op-amp model should be from the same catalog and company, transistors with lower base current should be preferred, adding an impedance matching circuit to the output layer of the proposed op-amp model or optimizing the load resistors in the output layer can be recommended. In the gain bandwidth test, which is one of the frequency parameters, it was observed that there was a sharp increase at very low frequencies in the traditional op-amp model, and this transition was smoother in the proposed op-amp model. In the maximum signal frequency determination test, it was observed that the operating region of the traditional op-amp model was increased. In the simulation studies, it was determined that the proposed op-amp model improved the regions where it crossovered at high frequency and low voltages compared to the traditional op-amp model. While the slew rate of the proposed op-amp model was $3.1V/\mu s$ in simulation studies, it was calculated as $2.95V/\mu s$ in experimental studies and $0.51V/\mu s$ and $0.68V/\mu s$ in traditional op-amp model, respectively. It was observed that slew rate of the proposed op-amp model was higher than that of the traditional op-amp model. It has been observed that the proposed op-amp model in the absolute maximum rated test, which is one of the unit parameters, works smoothly up to $\pm 22V$ at source voltages in both simulation and experimental environments. As for the total power consumption under these conditions, it has been seen that the proposed op-amp model consumes approximately the same power as the traditional op-amp model in simulation studies, but when the experimental results are compared, the proposed op-amp model consumes approximately %6 less power. Finally, when the rise and fall times of both op-amp models are examined in the test of the rise/fall times of the output signal, which is the switching parameter; it has been seen that the op-amp model with the fastest output response for use in switching circuits is proposed op-amp model. It was determined that the rise and fall times improved approximately 4 and 5 times, respectively. In experimental studies, it has been seen that the response time of the proposed op-amp model to the input signal at rise time is more advantageous than the traditional op-amp model, as in simulation studies. Considering the rise time, it was determined that the proposed op-amp model was approximately %25 slower than the traditional op-amp model, but despite this difference in rise time, the response time delay of the traditional op-amp model to the reference signal was slower than the proposed op-amp model. At the fall time, the proposed op-amp model was found to be approximately %14 faster than traditional op-amp model. Considering the response of the reference in signal on–off states, it was determined that the proposed op-amp model was faster, but when the rise and fall times were considered, traditional op-amp model was more advantageous. Also, the unpredictable parameters of the traditional op-amp model and modeling difficulties give an idea of the sensitivity of the proposed op-amp. This study presents important parameters in terms of preference op-amps according to usage

areas. It is expected that the proposed op-amp model will make significant contributions to the analog, digital and control circuits to be realized from now on.

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Declarations

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