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# A Low Power-Consumption Triple-Node-Upset-Tolerant Latch Design

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## Abstract

As the feature size of integrated circuit decreases, semiconductor devices become more susceptible to Single-Event-Upset (SEU) effect. This paper proposes a radiation hardened latch for Triple-Node-Upset (TNU) tolerance, which can block any triple node upset. Compared with previous radiation hardened TNU Tolerant (TNUT) latches, the proposed Low power-consumption TNUT (LTNUT) latch has the lowest power consumption. When compared with TNU Hardened Latch (TNUHL), TNUT Latch, TNU Completely Tolerant latch (TNUCT), Single-event Multiple-Node Upset Tolerant latch (SMNUT), TNU self-Recoverable Latch (TNURL), Low Cost and TNU-self-Recoverable Latch (LCTNURL) and Quadruple Dual Interlocked Storage Cell (Quadruple-DICE), the proposed LTNUT latch achieves reduction in power consumption by 30.77%, 17.11%, 40%, 20.25%, 20.25%, 27.59% and 64%, respectively. The proposed LTNUT latch achieves reduction in delay by 94.98%, 98.33%, 54.19%, 70.63% and 66.59% when compared with TNUHL, TNUT Latch, SMNUT, TNURL, LCTNURL, respectively, and introduces rise in delay by 3.38% and 5.52%, respectively, when compared with TNUCT and Quadruple-DICE. The proposed LTNUT latch has the lowest power consumption and second smallest delay. The proposed latch is not severely sensitive to temperature and voltage variations.

**Keywords** Latch · Triple node upsets · Radiation hardening · Block · Low power consumption

## 1 Introduction

The feature size of semiconductor devices is decreasing constantly, which improves the performance of integrated circuits greatly. Nevertheless, semiconductor devices are becoming more and more susceptible to single event effect correspondingly. Single event effect occurs when a high-energy particle strikes the sensitive node of the integrated circuit, which causes energy deposition and generates electron–hole pairs which will be collected by the sensitive node, to cause upset in circuits. In 1975, single event effect was first observed in integrated circuits [1]. Single event effect includes single event upset, single event transient, etc. Single event upset is divided into single node upset (SNU) and multiple node upsets (MNUs). SNU occurs when electron–hole pairs generated by particle strike are collected by a sensitive node and the logic value of sensitive node upsets. MNUs occur when particle striking upsets the logic values of multiple sensitive nodes under the effect of charge sharing. MNUs include double node upsets (DNUs) and triple node upsets (TNUs), etc. TNUs occurs when three internal nodes upset at the same time such as nodes (N5, N10, N15) in Fig. 9b. At present, the research on DNUs is mature; however, due to the aggressive process scaling, TNUs seriously affect the reliability of integrated circuits. In other words, the reinforcement technique for DNUs is no longer sufficient for aerospace applications that require high reliability. Therefore, there is a strong need to design high-reliability circuits to realize TNUs tolerance. Studies have shown that the single event effect is one of the

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main sources of faults in current spacecraft [2]. In 1982, a radiation hardened circuit against SNU was proposed [3]. In 2007, a radiation hardened circuit against DNUs was proposed [4]. In 2017, a radiation hardened circuit against TNUs was proposed [5]. Since then, more and more scholars have begun to pay attention to radiation hardened circuits [6–17]. Radiation hardened latches that can tolerate TNUs have been proposed, but they have large delay and power consumption, or small delay but large power consumption.

This paper proposes a radiation hardened Latch for Triple-Node-Upset Tolerance (LTNUT). LTNUT can block any TNUs by using ISEHL element which can self-recover from SEU and multi-level C-elements of its blocking characteristic [10]. LTNUT latch achieves reduction in power consumption by introduction of clocked inverter and clocked C-element. The LTNUT latch achieves reduction in power consumption by 31.42% on average, up to 64% when compared with the previous TNU-tolerant latches [5, 14, 19–23].

The rest of this paper is organized as follows. Section 2 introduces the basic elements commonly used in previous radiation hardened latches against TNUs. Section 3 introduces the schematic, working principle and radiation hardened principle of the proposed LTNUT latch. Section 4 compares the proposed LTNUT latch with previous latches in terms of radiation hardening ability, area, delay, power consumption, sensitivity to temperature and voltage variations. Section 5 concludes the paper.

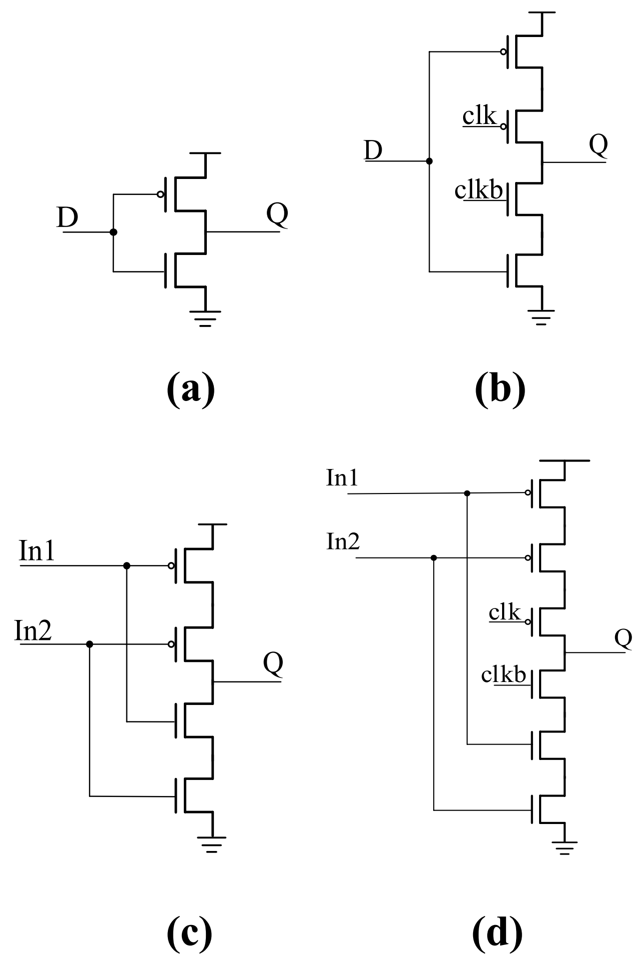



**Fig. 1** Commonly used basic elements **(a)** Inverter. **(b)** Clocked inverter. **(c)** Dual-input C-element. **(d)** Clocked dual-input C-element

## 2 Previous Hardened Latch Designs

### 2.1 Commonly Used Basic Elements

The basic elements commonly used in radiation hardened technology include inverters, clocked inverters, dual-input C-elements, clocked dual-input C-elements, etc. Their transistor-level schematics are shown in Fig. 1. The truth table of the dual-input C-element is shown in Table 1.

The working principle of the dual-input C-element is as follows. When the logic values of two inputs are same, the logic value of output is opposite to the logic values of inputs. When the logic values of two inputs are different, the output is in high impedance state and keeps the previous logic value unchanged. So, when one of the two inputs upsets, the dual-input C-element can block soft errors. Next section will introduce some radiation hardened latches against TNUs briefly.

### 2.2 Previous Radiation Hardened Latches

Figure 2 shows the schematic of a TNUHL latch. The latch consists of two storage elements and a clocked dual-input C-element. When TNUs occur, the error will be blocked by the storage element or the clocked dual-input C-element, so the TNUHL latch can block TNUs, but the blocking rate cannot reach 100%. The delay of TNUHL latch is large.

Figure 3 shows the schematic of a TNU-Latch. The latch is composed of C-elements and clocked C-elements. Through the blocking characteristic of the multi-level C-element, the TNU-Latch can block any TNUs with a large delay. Figure 4 shows the schematic of a TNUCT latch. The TNUCT latch consists of four clocked DICEs and three C-elements. Each clocked DICE can recover from SNU by

**Table 1** Truth table of the dual-input C-element

| In1 | In2 | Q |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | Hold |
| 1 | 0 | Hold |
| 1 | 1 | 0 |

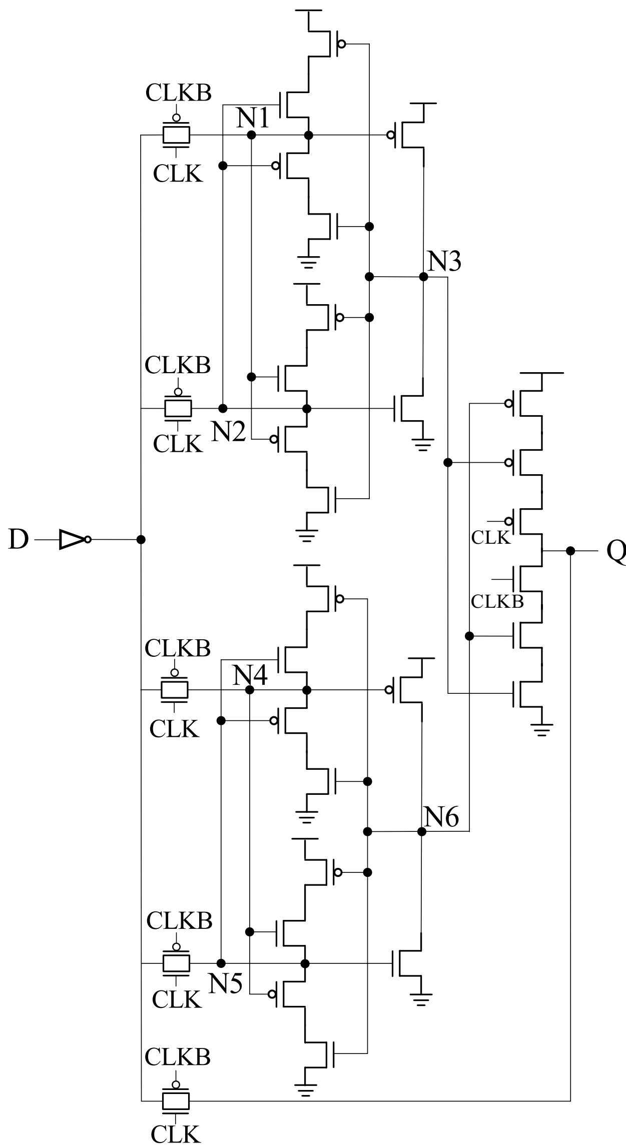



**Fig. 2** TNUHL

its self. The entire latch can realize TNUs tolerance. The TNUCT latch has good delay performance and small area overhead. Figure 5 shows the schematic of a SMNUT latch. The SMNUT latch uses three RFC elements, and the outputs of the three RFCs are 'wired-and' that used as final outputs. Each RFC element can achieve self-recovery from SNU, the SMNUT latch can tolerate any TNUs with low delay and power consumption. However, the SMNUT latch uses the 'wire-and' structure directly, which may generate short-circuit current and affect the normal operation of the circuit.

Figure 6 is the schematic of a TNURL latch that uses seven SIM elements. The SIM element consists of two three-input C-elements and a clocked dual-input C-element. The output of each SIM is fed back to the input of another SIM element. Through multiple feedbacks, TNURL can achieve

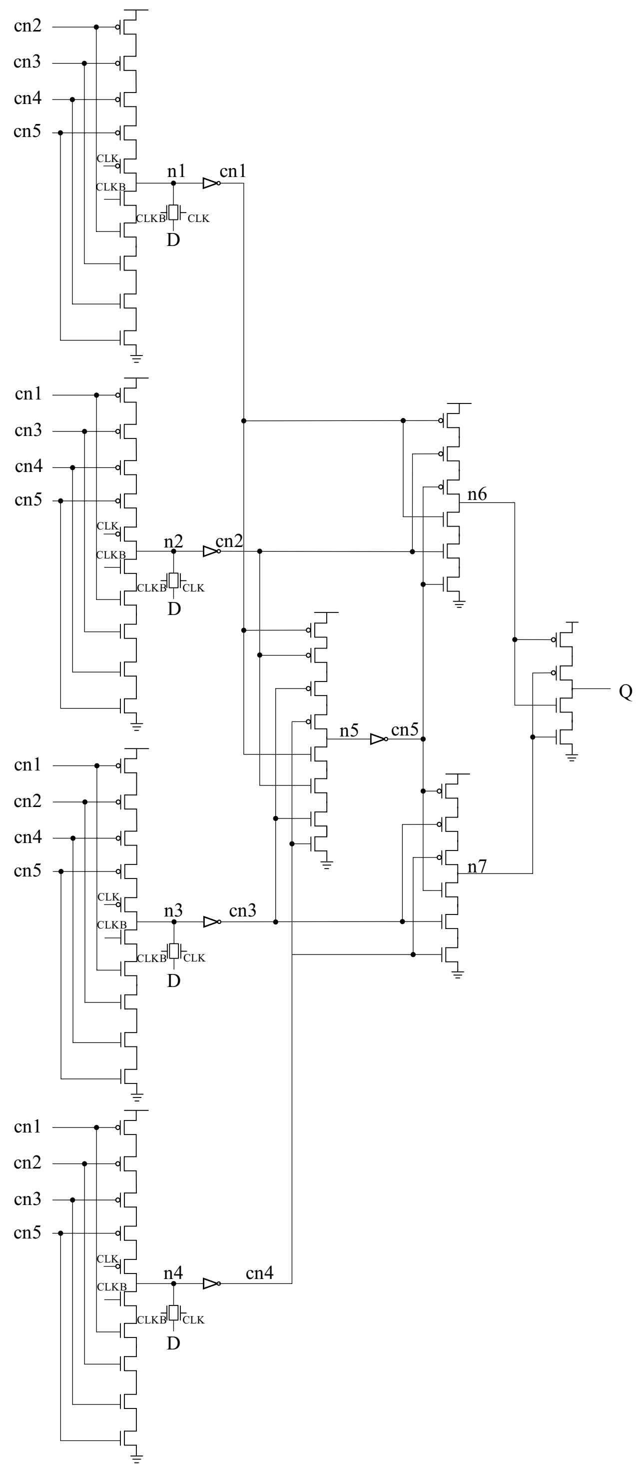



**Fig. 3** TNU-Latch

TNUs tolerance. However, due to the extensive use of SIM elements, the power consumption and delay of the TNURL latch are large. Figure 7 shows the schematic of a LCTNURL latch. Twelve three-input C-elements form a ring structure. The input and output of the C-elements are connected end

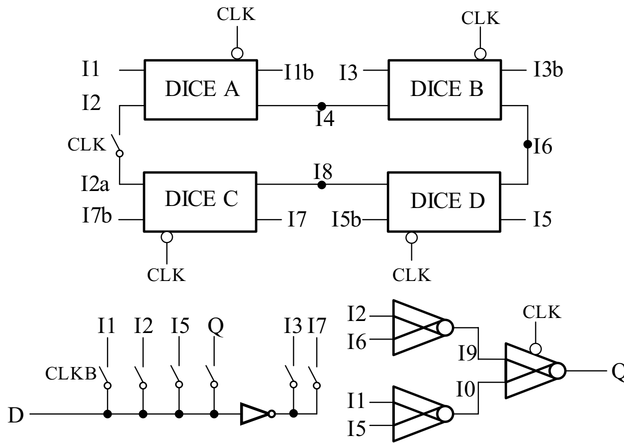



Fig. 4 TNUCT

to end to form a feedback loop. The LCTNURL latch can tolerate TNUs, but the delay and power consumption are relatively large. Figure 8 shows the schematic of a Quadruple-DICE latch. The Quadruple-DICE latch uses four DICEs and a clocked four-input C-element. Each DICE element can achieve self-recovery from SNU, and the clocked four-input C-element can block SNU that occurs on the internal node. Quadruple-DICE latch has low delay, but large power consumption.

## 3 Proposed Hardened Latch

Section 3 is organized as follows. Firstly, the schematic and working principle of the proposed LTNUT latch are explained. Secondly, the fault model will be introduced and the ability of radiation hardening will be validated by extensive fault injections in SPICE simulations.

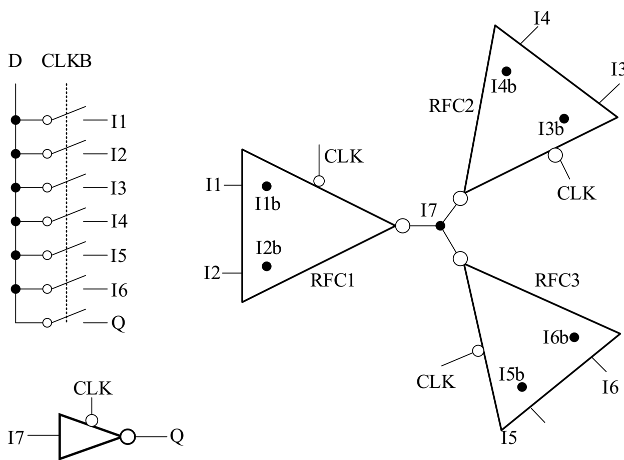



Fig. 5 SMNUT

### 3.1 Circuit Schematic and Working Principle

The proposed LTNUT latch is composed of the previous achievement of this laboratory ISEHL [9] element and dual-input C-elements. The ISEHL latch can fully protect all the internal nodes as well as output node against SEU regardless of the energy of particle strikes. It is suitable for low power circuits in which CG technology is applied to reduce power consumption. The idea of the multi-level c-elements work as a voter that can screen the right two nodes out of three when SEU happens and can block upset at node N5, N10, N15, N16, N17 [10, 27]. The use of the clocked C-elements can reduce the power consumption evidently during the transparent mode. Figure 9a shows the schematic of ISEHL latch that is composed of two inverters and three C-elements. The clocked inverters and clocked C-elements are utilized to reduce the power consumption. The working principle of ISEHL element is as follows. When CLK = 1 and CLKB = 0, the latch is in transparent mode, the two transmission gates are on, and the input data propagates to N1 and Q. When CLK = 0 and CLKB = 1, the latch is in holding mode, the two transmission gates are off, clocked inverter and clocked C-element are on, and the logic value of output Q is determined by the clocked C-element. The ISEHL element can self-recover from SNU and its working principle is as follows. When N1 is upset, the other input of the C-element maintains the correct value, so the upset at N1 is blocked. N3 will not be affected, so the output Q maintains the correct value. And N1 will restore to the correct logic value by N4. The principle against SNU of the remaining nodes is equivalent to that of N1. The SPICE simulations show that all the five internal nodes of the ISEHL element can recover from SNU by its self.

The schematic of the proposed LTNUT latch is shown in Fig. 9b. The working principle is as follows. When CLK = 1 and CLKB = 0, the latch is in transparent mode, the seven transmission gates are on, and the input data propagates to N1, N5, N6, N10, N11, N15, Q, the clocked C-element and the clocked inverter are off to reduce power consumption. When CLK = 0, CLKB = 1, the latch is in hold mode, the seven transmission gates are off, and the clocked C-elements and clocked inverters are on. The data saved by N1, N2, N3, N4, N6, N7, N8, N9, N11, N12, N13, N14 are maintained by C-elements and inverters. These data will propagate to N5, N10, and N15. Then the values of N5, N10, and N15 propagate to the output Q by two cascade C-elements and a clocked C-element.

### 3.2 Radiation Hardened Principles

Accurate fault injection model against single event effect is an important prerequisite for circuit-level simulation. This paper uses the double exponential current source model

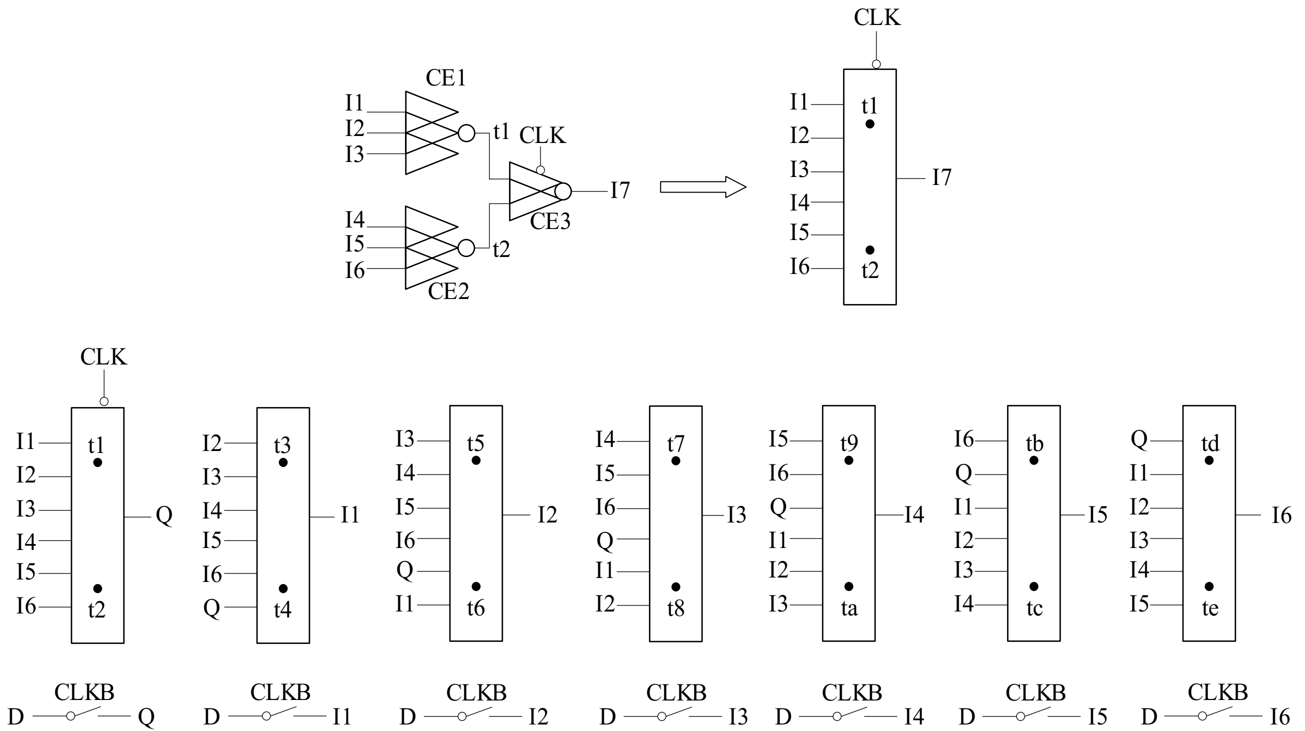



**Fig. 6** TNURL

[18]. Compared with the early single exponential current source model, the double exponential current source model can more accurately describe the process of rapid rise and slow decline of leakage current after particle incident It can be expressed by the following formula (1). Q is the amount of collected charge, $\tau_\alpha$ is the charge accumulation time constant. $\tau_\beta$ is the ion trajectory establishment constant. According to the parameters of references [7, 18, 26] and

**Fig. 7** LCTNURL

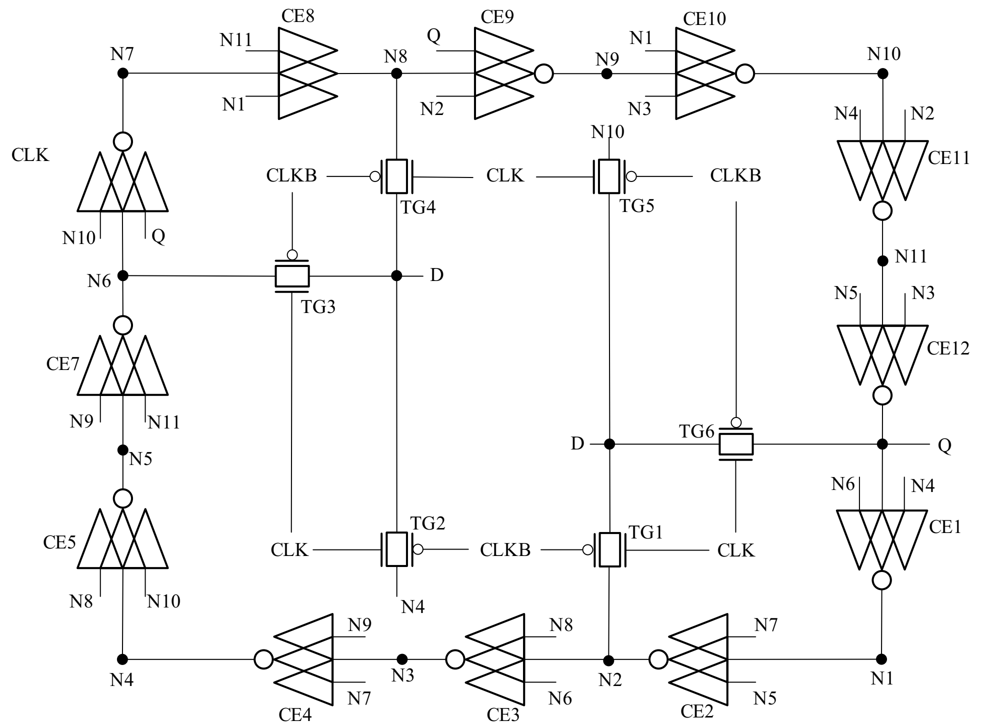
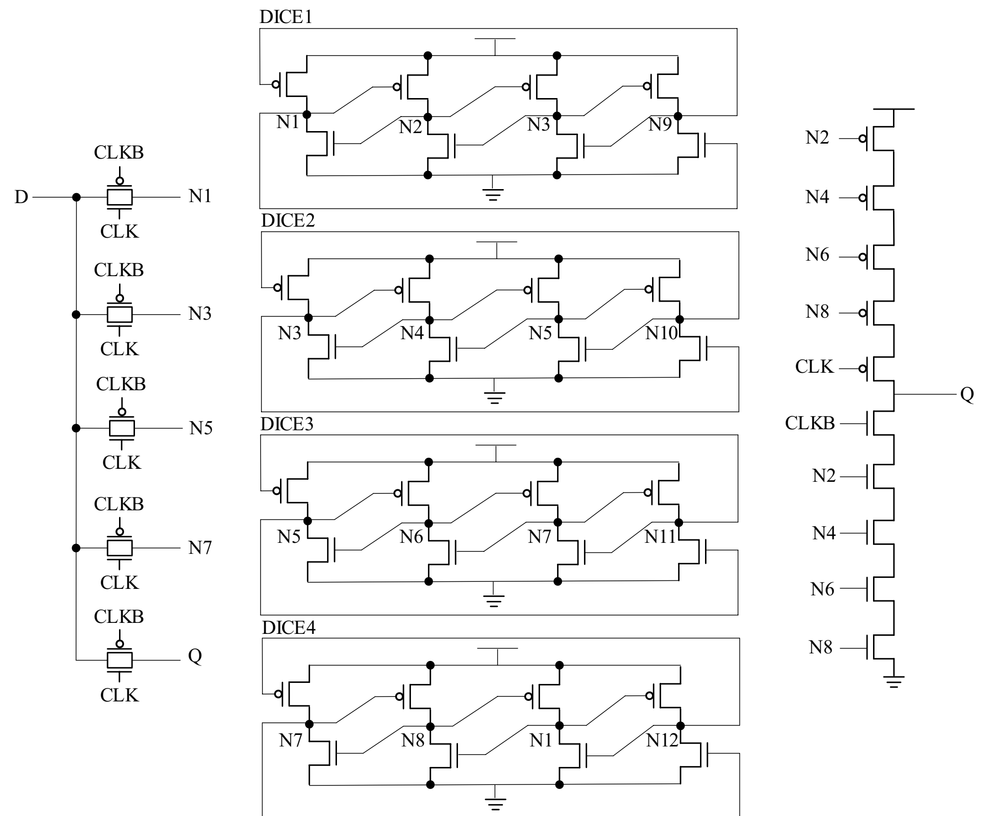


**Fig. 8** Quadruple-DICE




the simulation results, the value of $\tau_\alpha$ is 164 (ps) and the value of $\tau_\beta$ is 50 (ps).

$$I(t) = \frac{Q}{(\tau\alpha - \tau_\beta)} \times (e^{-t/\tau\alpha} - e^{-t/\tau\beta}) \quad (1)$$

The radiation hardened principles of proposed LTNUT latch will be introduced, in terms of a classification of SNU tolerance, DNUs tolerance, and TNUs tolerance.

**SNU tolerance:** Due to the symmetry of the schematic, Ni, Ni + 5 and Ni + 10 (i ≤ 5) are equivalent, so we only analyze the situation where SNU occurs at N1, N2, N3, N4, N5, and N16. When N1 upsets, the logic value of the other input N5 of C-element remains unchanged, so other nodes will not be affected, and N1 will restore by the unaffected N4. N2 is equivalent to N1. When N3 upsets, N2 will upset too, and then the soft error will be blocked by the C-element, and N3 will restore to the correct logic value by C-element. N4 is equivalent to N3. When N5 upsets, the logic value of the other input N10 of the C-element remains unchanged, so the other nodes are not affected, and N5 will restore the correct value by C-element. N16 is equivalent to N5. It can be seen that the LTNUT latch can tolerate all SNU situations. Figure 10 shows the waveforms of SNU injections Figs. 11, 12.

**DNU tolerance:**the discussion is divided into the following three situations: case1: no ISEHL element is affected; case2: one ISEHL element is affected; case3: two ISEHL element are both affected.

**Case1:** There is one situation in this case. Both N16 and N17 are affected, output Q will upset at this time, but N5, N10, and N15 are not affected, so N16 and N17 restore the correct logic value, then the output Q restores the correct value.

**Case2:** There are 60 situations in this case and can be divided into two situations specifically. (a): Both the two nodes are in the same ISEHL element;(b): One of the nodes in N16 or N17 is affected, and one node in ISEHL element is affected.

a) There are 30 situations in this case. At this time, the other two ISEHL elements are not affected, the error will be blocked by the C-element, so LTNUT latch can block DNUs. For example, when <N1, N2> upsets, N3 and N4 are not affected, N5 outputs the correct logic value, output Q maintains the correct logic value.
b) There are 30 situations in this case. At this time, the ISEHL element can self-recover from SNU, even if the N16 or N17 upsets, ISEHL element will still be recovered. For example, when <N5, N16> upsets, the error

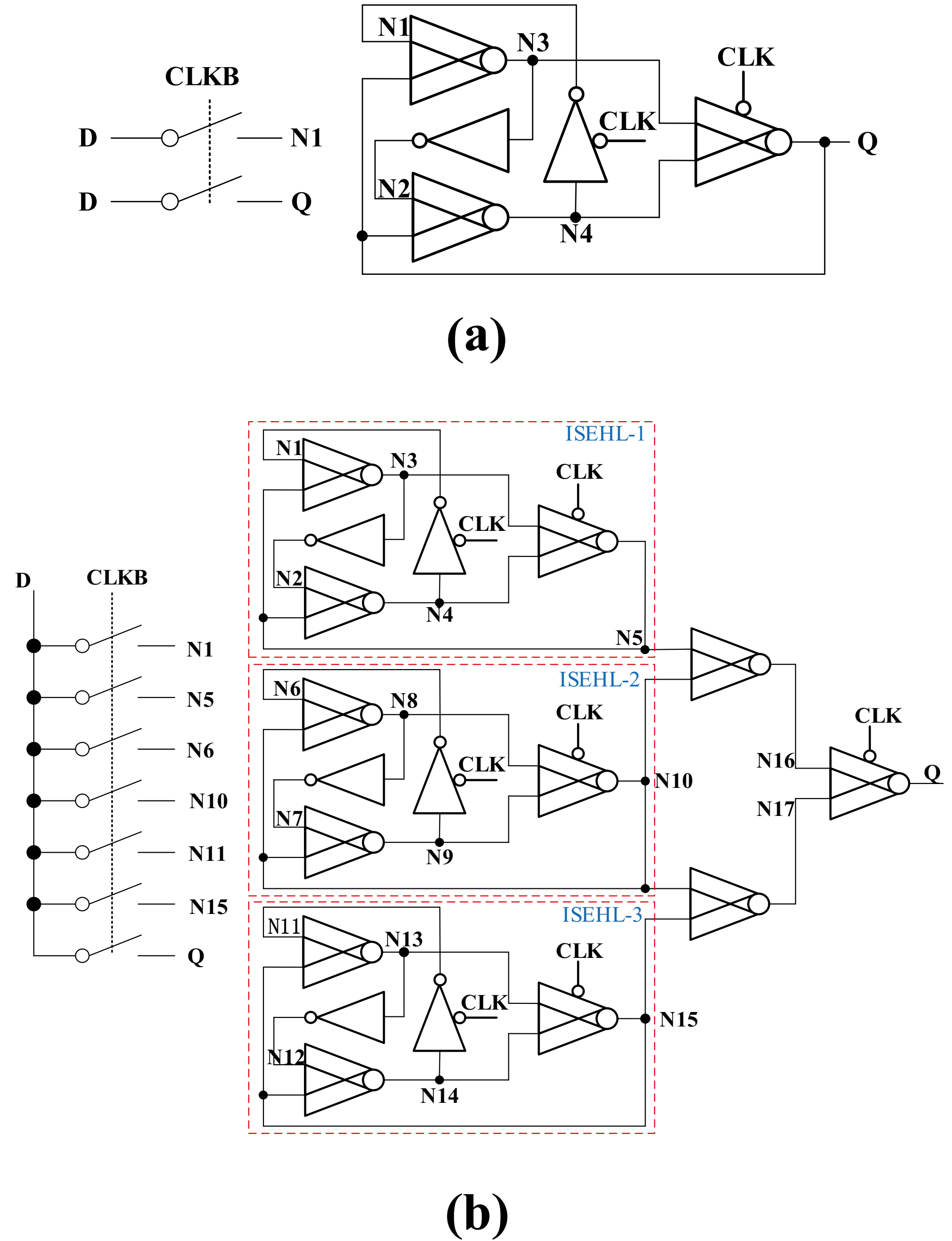



**Fig. 9** Schematics (**a**) Schematic of ISEHL (**b**) Schematic of proposed LTNUT latch

at N5 will be blocked by C-element, and N5 will restore correct logic value by N3 and N4. The error at N16 will be blocked by the C-element and N16 will restore to the correct logic value by N5 and N10, output Q will maintain the correct logic value.

**Case3:** There are 75 situations in this case. When two ISEHL elements suffer SNU respectively, both of the two ISEHL elements will self-recover, so that no error will propagate to the output node. For example, when <N5, N10> upsets, the error will propagate to N16, and then blocked by the C-element, and output Q maintains the correct logic value.

**C.TNUs tolerance:** There are 680 situations of TNUs totally. LTNUT has seventeen internal nodes, the total situations of TNUs come from the following calculation:

$$C_{17}^{3} = 680$$

The discussion is divided into the following situations: case1: one ISEHL element is affected; case2: two ISEHL elements are affected; case3: three ISEHL elements are affected.

**Case1:**There are 105 situations in this case and can be divided into three situations specifically. (a): Three nodes

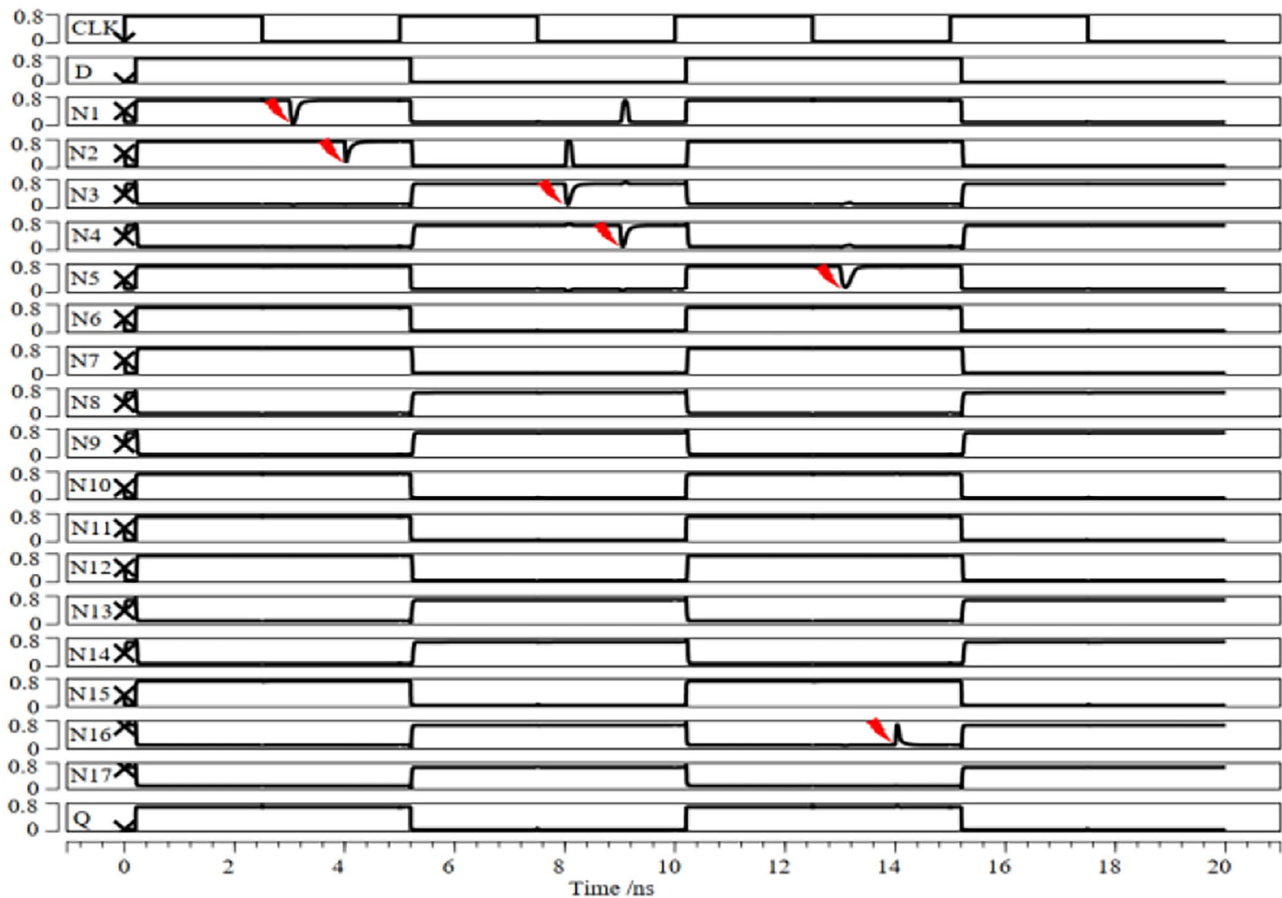



**Fig. 10** Waveforms of proposed latch with SNU injections

in the same ISEHL element are affected; (b): Two nodes in one ISEHL element are affected, one node of N16 and N17 is affected; (c): one node in one ISEHL element is affected, both N16 and N17 are affected.

a) There are 30 situations in this case. At this time, only one ISEHL element is affected while the other two ISEHL elements working normally. The error will be blocked by the C-element, and the output will not be affected. For example, when <N1, N2, N5> upsets, the error at N5 will be blocked by the C clement and output Q will maintain the correct logic value.
b) There are 60 situations in this case. At this time, the unaffected ISEHL element will restore the N16 or N17 to normal or block the error, so the output will not be affected even if one ISEHL element is affected. For example, when <N3, N5, N17> upsets, N10, N15, and N16 are not affected, errors at N5 and N17 will be blocked by the C-element. Output Q maintains the correct logic value.
c) There are 15 situations in this case. At this time, only one ISEHL element is affected, and the error that occurs will recover, which is equivalent to a DNUs situation that both N16 and N17 nodes upset. The output will be affected temporarily, and then restores to the correct logic value. For example, when <N5, N16, N17> upsets, Q will upset too. But N5 will restore to the correct logic value, so that N16 and N17 will restore the correct logic value under the action of C-elements. Output Q will restore the correct logic value.

**Case2**: There are 450 situations in this case totally and can be divided into two situations specifically:(a): two ISEHL elements suffer SNU respectively, and one of the N16 or N17 is affected (b): Two upset nodes belong to different ISEHL elements.

a) There are 150 situations in this case. At this time, the error in the ISEHL element will self-recover, and the error at N16 or N17 will not affect the output Q. For example, when <N5, N10, N16> upsets, the error at N16 will be blocked by the C-element, N5 and N10 will restore to the correct logic value, so that N16 will restore the correct logic value. Output Q will maintain the correct logic value.

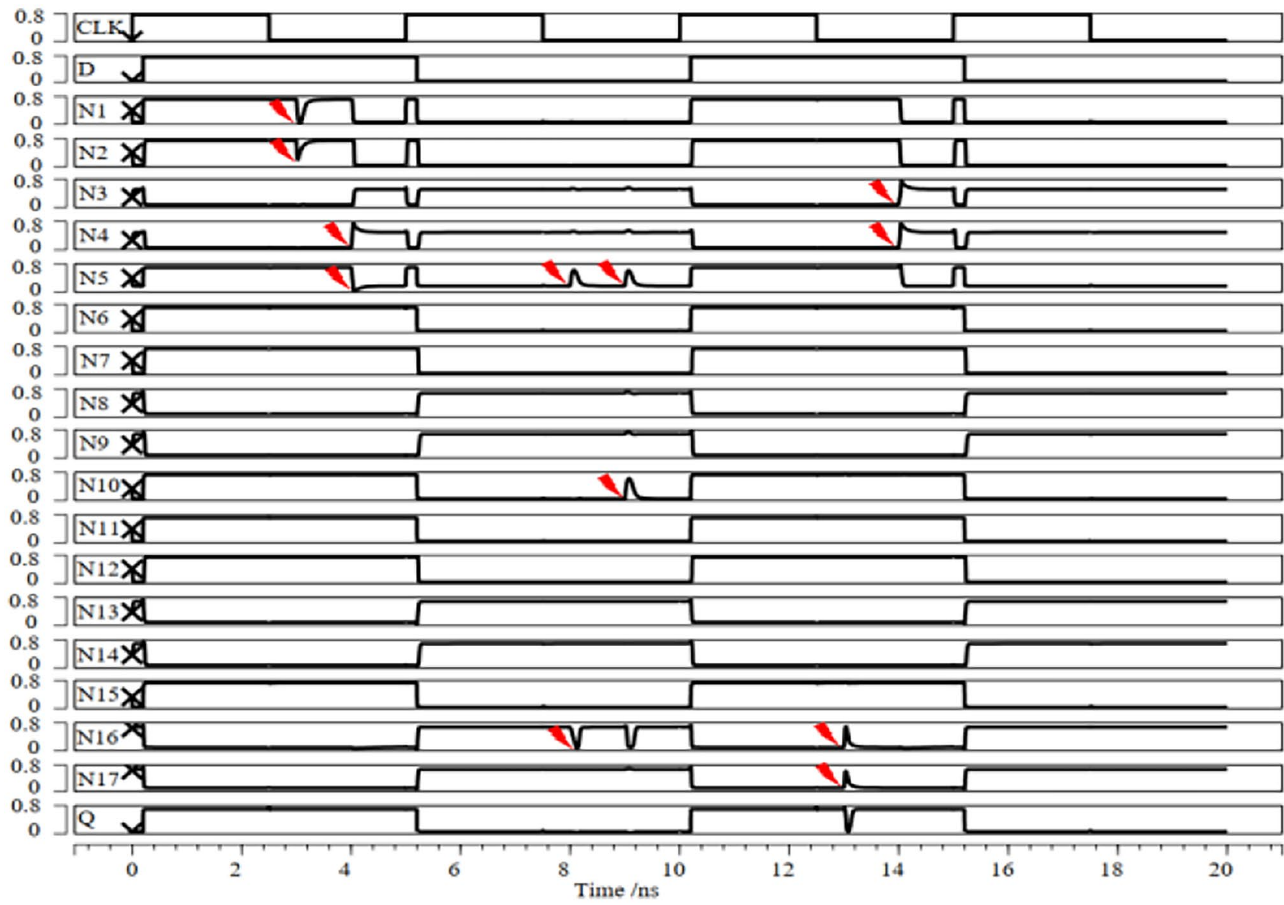



**Fig. 11** Waveforms of proposed latch with DNUs injections

b) There are 300 situations in this case. The output of the ISEHL element that suffers DNUs is wrong while the other two ISEHL elements still output the correct logic value, so the output will not be affected. For example, when < N3, N4, N10 > upsets, N5 and N16 upset, and the error at N16 will be blocked by the C-element. Output Q will maintain the correct logic value.

**Case3:** There are 125 situations in this case. All the three ISEHL elements suffer SNU, but can self-recover totally, output Q will not be affected. For example, when < N5, N10, N15 > upsets, N16, N17, and Q will upset, but N5, N10, and N15 will self-recover overall. So that N16, N17, and Q will recover to the correct logic values.

## 4 Performance Evaluation

This section will compare the proposed LTNUT latch with previous latches, in terms of radiation hardened ability, performance, overhead, and sensitivity to temperature and voltage variations. All latches are simulated with PTM 22 nm technology. All transistors have the same aspect ratio, the clock signal CLK and complementary clock signal CLKB are given by excitation. The simulation software used is HSPICE.

### 4.1 Comparison of Radiation Hardened Ability

As shown in Table 2, the proposed latch compares with previous latches in terms of radiation hardened ability. The evaluation indicators are SNU blocking, SNU self-recovery, DNUs blocking, DNUs self-recovery, and TNUs blocking. Blocking means that the latch will block the propagation of SEU/DNUs/TNUs, the output will still maintain the correct logic value; Self-recovery means that the latch will recover to the initial logic value when SEU/DNUs/TNUs occur. The proposed LTNUT latch can effectively achieve TNUs blocking ability.

### 4.2 Performance and Area Comparison

Table 3 shows the proposed LTNUT latch and previous hardened latches in terms of delay, power consumption, area and

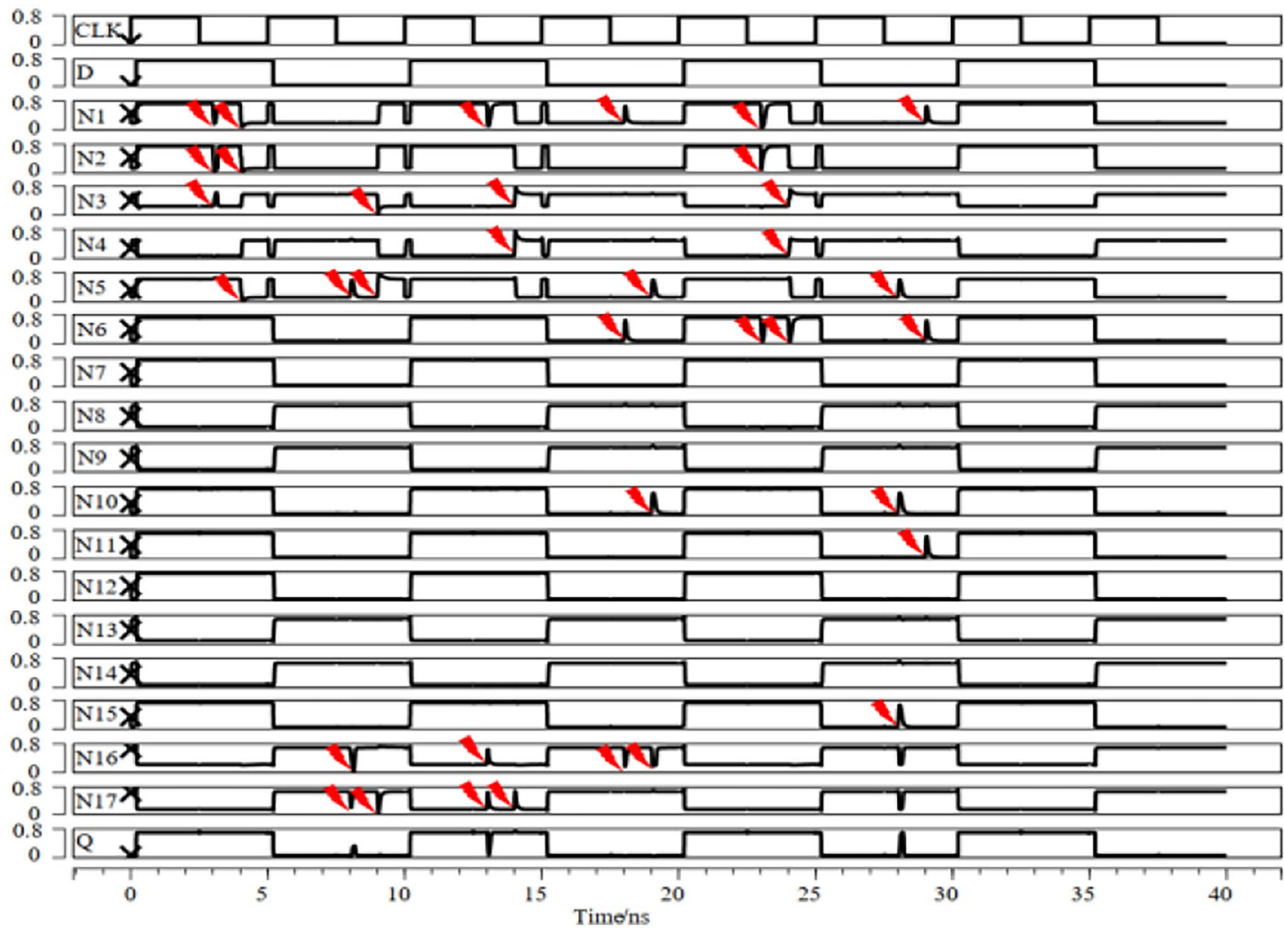



**Fig. 12** Waveforms of proposed latch with TNUs injections

**Table 2** Comparison of radiation hardened ability

| | Latches | SNU blocking | SNU Self-recovery | DNUs blocking | DNUs Self-recovery | TNUs blocking |
|---|---|---|---|---|---|---|
| SNU | HLR [6] | √ | × | × | × | × |
| | SIN-LC [7] | √ | × | × | × | × |
| | SIN-HR [7] | √ | × | × | × | × |
| | STC [8] | √ | × | × | × | × |
| | ISEHL [9] | √ | √ | × | × | × |
| | DICE [11] | √ | √ | × | × | × |
| | HPST [12] | √ | × | × | × | × |
| DNUs | DELTA-DICE [13] | √ | √ | √ | √ | × |
| | DNUCT [14] | √ | √ | √ | × | × |
| | HRDNUT [15] | √ | √ | √ | √ | × |
| | DONUT [16] | √ | √ | √ | √ | × |
| | NTHLTCH [17] | √ | √ | √ | √ | × |
| TNUs | **proposed** | √ | √ | √ | √ | √ |
| | SMNUT [19] | √ | √ | √ | √ | √ |
| | TNURL [20] | √ | √ | √ | √ | √ |
| | LCTNURL [21] | √ | √ | √ | √ | √ |
| | TNUCT [14] | √ | √ | √ | √ | √ |
| | Quadruple-DICE [22] | √ | √ | √ | √ | √ |
| | TNUHL [23] | √ | √ | √ | √ | √ |
| | TNU-Latch [5] | √ | √ | √ | √ | √ |

**Table 3** Performance and Area Comparison

| | Latches | Delay (ps) | Power (uW) | Area (USTs) | PDP (aJ) |
|---|---|---|---|---|---|
| SNU | HLR [6] | 1.51 | 0.21 | 72 | 0.32 |
| | SIN-LC [7] | 5.1 | 0.17 | 30 | 0.87 |
| | SIN-HR [7] | 4.2 | 0.21 | 42 | 0.88 |
| | STC [8] | 32.05 | 0.29 | 42 | 9.29 |
| | ISEHL [9] | 2.86 | 0.19 | 72 | 0.54 |
| | DICE [11] | 11.22 | 0.51 | 56 | 5.72 |
| | HPST [12] | 2.24 | 0.45 | 84 | 1.00 |
| DNUs | DELTA-DICE [13] | 13.72 | 0.96 | 114 | 13.17 |
| | DNUCT [14] | 1.6 | 1.19 | 204 | 1.90 |
| | HRDNUT [15] | 4.03 | 0.44 | 132 | 1.77 |
| | DONUT [16] | 24.06 | 1.75 | 102 | 42.11 |
| | NTHLTCH [17] | 12.38 | 1.20 | 180 | 14.86 |
| TNUs | **proposed** | **1.53** | **0.63** | **264** | **0.96** |
| | SMNUT [19] | 3.34 | 0.79 | 234 | 2.64 |
| | TNURL [20] | 5.21 | 0.79 | 420 | 4.12 |
| | LCTNURL [21] | 4.58 | 0.87 | 252 | 3.98 |
| | TNUCT [14] | 1.48 | 1.05 | 228 | 1.55 |
| | Quadruple-DICE [22] dsdddDICEDICE | 1.45 | 1.75 | 156 | 2.54 |
| | TNUHL [23] | 30.5 | 0.91 | 114 | 27.76 |
| | TNU-Latch [5] | 91.44 | 0.76 | 240 | 69.49 |

PDP. Delay refers to the propagation delay from input D to output Q during the transparent mode. Power consumption refers to the average power consumption of the circuit within 20 ns under the same starting configuration. Area overhead is measured by the number of Unit Size Transistors (USTs) [24].

The relationship between area overhead and USTs is shown in formula (2). The PDP is the product of power consumption and delay, which can evaluate the performance of the circuit comprehensively. The smaller is the PDP, the better is the performance.

$$USTs = \sum_{i=1}^{n} (W/L)_i \tag{2}$$

As we can see from Table 3, the proposed LTNUT latch achieves reduction in delay and power consumption by 53.69% and 31.42% on average respectively when compared with other TNUs tolerant latches. The proposed LTNUT latch has the lowest power consumption and PDP with the same radiation hardened ability.

### 4.3 Variation Sensitivity Analysis

The feature size of integrated circuits scales continuously with the continuous progress of science and technology. Temperature and voltage variations have a greater and greater impact on the reliability of nano integrated circuits [25]. In this paper, the power consumption and delay of some TNUs tolerant latches under temperature and voltage variations are measured.

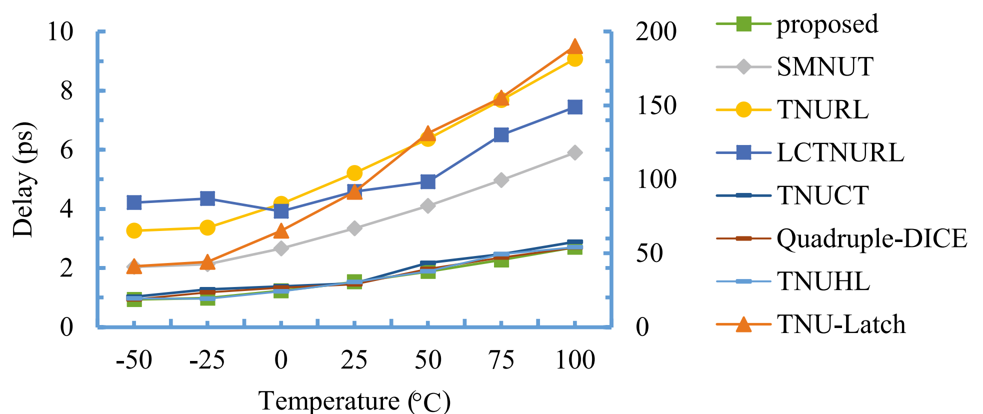



**Fig. 13** Delay variation of latches at different temperatures

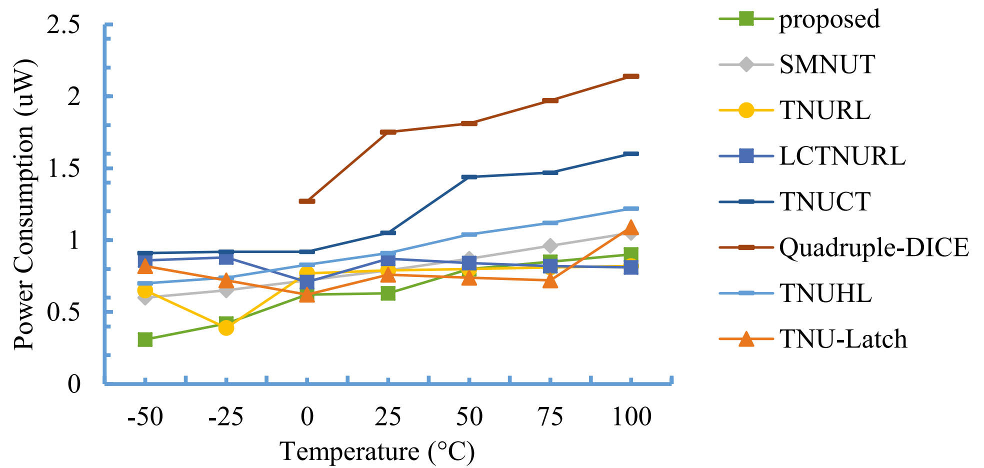



**Fig. 14** Power consumption variation of latches at different temperatures

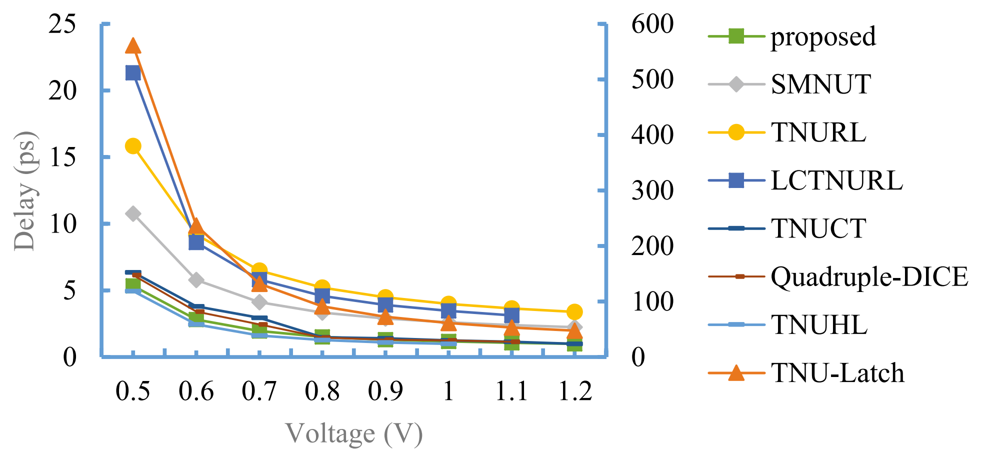



**Fig. 15** Delay variation of latches at different voltages

Figures 13, 14 show the power consumption and delay variations of each latch at different temperatures respectively. In Fig. 13, TNUHL and TNU-latch correspond to the secondary coordinate axis on the right. The other latches correspond to the left coordinate axis. The temperature variation range is -50 ℃ ~ 100 ℃ and the step is 25 ℃. As can be seen from the Figs. 13, 14, the delay and power consumption of the latches show a rising trend as the temperature increases. The delay variation of the proposed LTNUT at different temperatures is smoothest and the power consumption variation is moderate.

Figures 15, 16 show the power consumption and delay variations of each latch at different voltages respectively. TNUHL and TNU-latch correspond to the secondary coordinate axis on the right, and the other latches correspond to the left coordinate axis in Fig. 15. The voltage variation range is 0.5 V ~ 1.2 V and the step is 0.1 V. As can be seen from the Figs. 15, 16, as the voltage increases, the delay of the latches shows a falling trend while the power consumption shows a converse trend on the whole. The delay variation of proposed LTNUT latch under different voltages is smoothest and the power consumption variation is moderate.

To compare the performance of different latches under temperature and voltage variations more accurate, the variance of temperature and voltage variations of different latches are measured. Table 4 shows the variance of temperature and voltage variations of different latches. $\sigma^2$(TD) shows the variance of delay variation at different temperatures; $\sigma^2$(TP) shows the variance of power consumption variation at different temperatures; $\sigma^2$(VD) shows the variance of delay variation at different

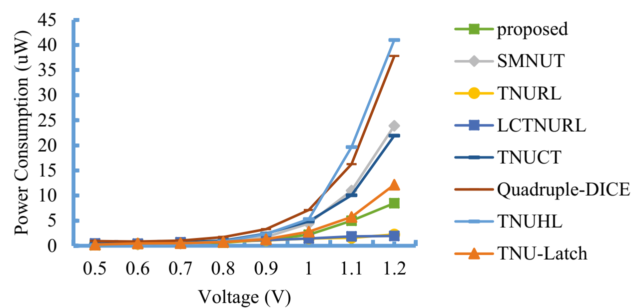



**Fig. 16** Power consumption variation of latches at different voltages

**Table 4** Variance of temperature and voltage variations of different TNU hardened latches

| Latches | $\sigma^2$(TD) | $\sigma^2(TP)\times 10^2$ | $\sigma^2$(VD) | $\sigma^2$(VP) | Average variance |
|---|---|---|---|---|---|
| **proposed** | **0.45** | **4.91** | **2.17** | **8.76** | **2.86** |
| SMNUT [19] | 2.17 | 2.69 | 8.25 | 69.6 | 20.01 |
| TNURL [20] | 4.94 | 2.43 | 17.77 | 0.477 | 5.807 |
| LCTNURL [21] | 1.75 | 0.33 | 42.00 | 0.35 | 11.03 |
| TNUCT [14] | 0.48 | 9.21 | 3.52 | 56.14 | 15.06 |
| Quadruple-DICE [22] | 0.47 | 10.68 | 3.34 | 166.08 | 42.50 |
| TNUHL [23] | 198.67 | 3.85 | 1303.67 | 212.69 | 428.77 |
| TNU-Latch [5] | 3326.06 | 2.21 | 30,540.62 | 17.10 | 8470.95 |

voltages; $\sigma^2$(VP) shows the variance of power consumption variation at different voltages; The $\sigma^2$(TD), $\sigma^2$(VD) and average variance of proposed LTNUT latch are smallest. It shows that the proposed latch has the smallest temperature and voltage variations when compared with other comparative latches.

## 5 Conclusion

With the rapid development of nanoscale integrated circuits, reliability has become a serious issue. This paper presents a low overhead latch for TNUs blocking. The proposed latch integrates clocked C-element and clocked inverter to reduce the power consumption. Cascade and feedback scheme can effectively improve the reliability. In this paper, PTM22nm process is used. Extensive SPICE simulations show that the proposed LTNUT latch can block any SNU/DNUs/TNUs. The proposed LTNUT latch has the lowest power consumption and sub-optimal delay performance. The latch has a large area overhead but the lowest PDP by its low delay and power consumption. When the latch is in the holding mode, all C-elements and inverters are on to ensure the latch work properly, but when the latch is in the transparent mode, the clocked C-elements and clocked inverters are skillfully off, so as to reduce the power consumption. At the same time, the input D can transfer to Q by transmission gate with a low delay. The proposed LTNUT latch can reduce delay, power consumption and PDP significantly when compared with previous latches with equivalent TNUs blocking ability and has the lowest sensitivity to temperature and voltage variations.

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