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Impact of Fin-Height on SRAM Soft Error Sensitivity and Cell Stability

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Abstract FinFET technology has become the most promising alternative to continue CMOS scaling due to its improved short channel effects. Design flexibility reduces on FinFET based circuits such as SRAM cells due to the effective channel width is determined by an integer number of fins. In this work, the impact of fin height size of FinFET transistors on the simultaneous behavior of soft error sensitivity and SRAM cell static noise margin is investigated. 3-D TCAD Sentarus environment is used to quantify the amount of collected and critical charges of an SRAM cell due to a heavy ion strike while Mix-Mode Hspice-TCAD simulation is used for stability analysis. Even more, the influence of process variations on sensitivity to soft errors and cell stability is considered. A 10 nm-SOI Tri-Gate FinFET technology is used. Results show that increasing the fin height of FinFET transistors considerably increases SRAM cell sensitivity to soft errors but improves its stability. This suggests that the optimum fin height value of FinFET transistors of an SRAM cell depends on the best tradeoff between soft error robustness and stability.

Keywords FinFET · Soft errors · Static noise margin · Process variations

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1 Introduction

Traditional CMOS scaling beyond the 22 nm technology node is severely constrained by *short channel effects* and process variations due to *Random Dopant Fluctuations* (RDF). FinFET technology projects as a promising candidate to continue CMOS scaling. FinFET devices have a stronger electrostatic control over the channel due to the gate wraps around a thin slice of silicon, which is known as *fin*. Hence, high channel doping is not required in FinFETs decreasing the threshold voltage variations due to RDF [10]. Besides, one of the major circuit design differences using FinFET or CMOS planar is that the width of FinFET devices is quantized by increasing the number of fins of the device. This unique feature of FinFETs reduces design flexibility of SRAM cells which may pose performance issues.

There is s strong interest for better understanding SRAMs cell stability and its sensitivity to radiation effects in FinFET technology. There is a little work published about the impact of fin height on SRAM cell stability and sensitivity to radiation. Even more the influence of process variations needs to be properly addressed.

Alpha particles from the packaging materials, high energy neutrons from cosmic radiations and the interaction of cosmic ray thermal neutron are three major sources of radiation inducing soft errors [1]. In SRAM cells a soft error is typically due to *Single Event Upset* (SEU), and occurs when a particle strikes at a storage node in the cell inducing a transient voltage pulse that causes a bit flip in the SRAM cell. In [7] a relative soft-error rate (SER) of bulk FinFET SRAM cell was compared with planar SRAM cells by using TCAD simulations. In [14, 17] 3-D TCAD simulations were employed to model the response to radiation of FinFETs. In addition, Munteanu et al. [13] showed that 3T-FinFET and 3T-Multi-channel nano-wires have better radiation hardness

than conventional fully-depleted single-gate SOI transistors. In [16], alpha-particle and cosmic ray induced SER benefits of 22 nm high-K and metal-gate bulk Tri-Gate devices have been measured and compared against equivalent devices manufactured in a 32 nm planar bulk CMOS technology. It is shown that tri-gate devices present better benefits to single event upset (SEU) scaling.

Static Noise Margin (SNM) is the most used metric to quantify the stability of an SRAM cell. In [6] the SNM of a FinFET SRAM cell was investigated operating in sub-threshold region. An analytical SNM model validated by 3-D TCAD analysis was presented. In [8], the stability, performance, and variability of 6T FinFET SRAM cells with asymmetric gate-to-source/drain underlap devices are analyzed. In [4], a novel multiple fin height technology was used for 10 nm Si-based bulk FinFETs 6T SRAM cell. They found that this technology presents 25 % better SNM at 0.6 V than single fin-height baseline.

The main goal of this paper is to investigate the impact of fin height sizing of FinFET transistors on the simultaneous behavior of soft error sensitivity and SRAM cell static noise margin. Even more, the influence of process variations is analyzed. The charge collection mechanism of a FinFET-based SRAM cell due to a heavy ion strike has been analyzed using 3-D TCAD Sentaurus simulations. SNM of a FinFET-based SRAM cell is analyzed with the ”butterfly” curve of the SRAM cell obtained with mix-mode Hspice-TCAD simulations. Results are presented for a 10 nm-SOI Tri-Gate FinFET technology. Multiple-node charge collection mechanism is considerably lower in SOI technologies than in bulk technologies [3], therefore, this effect has not been considered in the present work.

The rest of the paper is organized as follows: Section 2 presents the basics about the FinFET transistor, and process variation modeling. In Section 3, the SRAM cell behavior under an ion strike is analyzed. In Section 4, the impact of fin height on SRAM cell stability is analyzed. Finally, the conclusions of the work are given in Section 5.

2 FinFET Transistor and Process Variation Modeling

2.1 FinFET Transistor

Figure 1 illustrates the physical structure of a SOI Tri-Gate FinFET transistor. The gate wraps around a thin slice of silicon, which is known as *fin*. *L* is the channel length, *HFIN* is the fin height, *TFIN* is the fin thickness, *TOX* is the oxide thickness and *TBOX* is the buried oxide thickness.

Since the gate wraps around the silicon *fin*, this results in three channel sides: two sidewall channels and a top channel, as shown in Fig. 2. The transistor current flows along

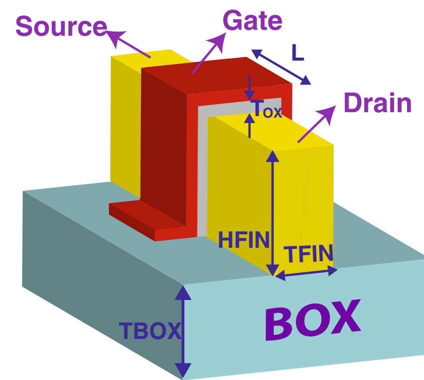


Fig. 1 Tri-gate FinFET device

the top and side surfaces of the fin: I_{DS1} and I_{DS2} represent the drain currents flowing at the sidewalls of the fin, and I_{DS3} represents the drain current flowing at the top of the fin. Thus, the effective channel width (W_{eff}) of a Tri-Gate FinFET transistor is given by,

$$W_{eff} = NFIN \times (2HFIN + TFIN) \quad (1)$$

where *NFIN* is the number of fins and can only take integer values.

The fin's dimensions play a key role in defining the operation of the device. Wider fin structures behave more like planar devices. In narrower fin devices, the additional lateral gates provide better control over the body. This significantly mitigates the short channel effects. Moreover, the lateral gates allow further scaling of the FinFET transistor with a relatively thicker gate oxide in comparison to a planar structure. This reduces the gate tunneling leakage current and improves the drive current capability of the FinFET device.

2.2 Process Variation Modeling

Local and global variations in *gate work function (WF), channel length (L), fin thickness (TFIN), fin height (HFIN) and oxide thickness (TOX) have been considered.* Local variations of individual transistors within SRAM cell are uncorrelated while global variations of cell transistors are

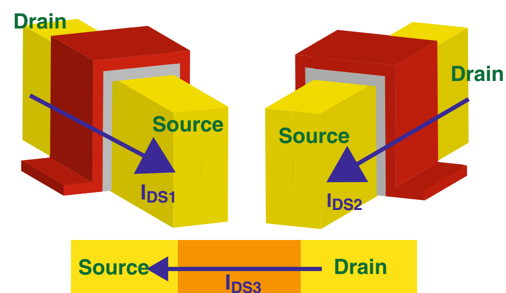


Fig. 2 Tri-gate FinFET current

correlated. WF local variation is due to metal gate granularity, which is independent for each transistor. WF variation is assumed to have a Gaussian distribution with σ_{WF}=20meV [2]. Local variation for L and TFIN is due to *Line Edge Roughness*. *Gate LER* (known as GER) is defined for L variation, and *Fin LER* (known as FER) is defined for TFIN variation.

Normal distributions have been assumed to model GER and FER variations with $\sigma_{GER,FER} = 0.66\ nm$ [18]. HFIN and TOX are not expected to exhibit significant local variation since they are determined by film thickness, but not the lithography [11]. Global variation is assumed to be 3σ=10 % from the nominal value for each parameter. Monte Carlo simulations have been carried-out to obtain statistical distributions for the design metrics. A process parameter is denoted by P, which is calculated using the following expression:

$$P_{ij} = P_{nominal} + \Delta P_{Global,j} + \Delta P_{Local,ij} \quad (2)$$

P_{ij} denotes the parameter value for the ith transistor during the jth Monte Carlo run. $P_{nominal}$ is the nominal value of the parameter. The global variation component $\Delta P_{Global,j}$ is generated for each Monte Carlo run and applied to all transistors in the FinFET SRAM cell. The local variation component $\Delta P_{Local,ij}$ is generated for each transistor for each Monte Carlo run.

3 Impact of Fin Height on Soft Error Sensitivity

In this section, a FinFET-based SRAM cell under an heavy ion strike is analyzed.

3.1 SRAM Cell Behavior Under an Ion Strike

3.1.1 Behavior of 6T-FinFET SRAM Cell Under a Heavy Ion Strike

Figure 3 shows the circuit schematic of the basic six transistors FinFET-based SRAM cell. *Mp1* and *Mp2* are the pull-up transistors, *Mn1* and *Mn2* are the pull-down transistor, and *Ma1* and *Ma2* are the access transistors. *A* and *B* are the

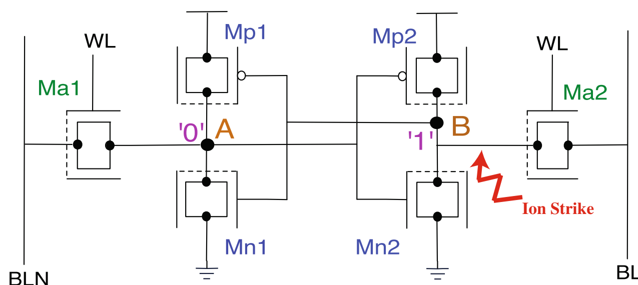
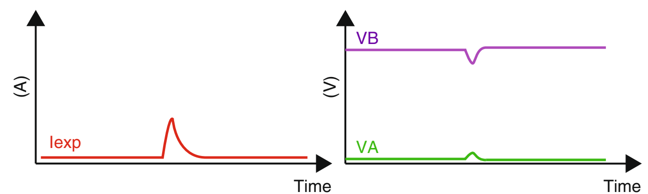
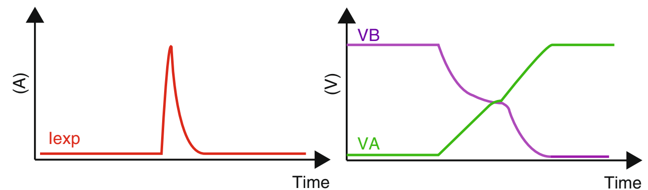


Fig. 3 FinFET SRAM cell



(a) $Q_{coll} < Q_{crit}$. Nobit-flip occurs.



(b) $Q_{coll} > Q_{crit}$. Bit-flip occurs.

Fig. 4 SRAM transient response due to a heavy ion strike

storage nodes. Assume a heavy ion strikes node *B* where a logic '1' is stored. When an ion strike occurs, electron-hole pairs (EHPs) are generated in the silicon fin which end up collected at the drain terminal of transistor *Mn2* giving rise to a transient current from drain to the body. This is shown in Fig. 4 where I_{exp} is the current generated from drain to body. Its amplitude and duration are defined by the amount of the collected charge (Q_{coll}) at the drain terminal. If the collected charge at node *B* is small, no bit-flip occurs as shown in Fig. 4a. However, if the collected charge is larger than a threshold value (critical charge - Q_{crit}), the SRAM flips (See Fig. 4b). This is known as Single Event Upset (SEU).

3.1.2 Simulation Setup at 3-D TCAD Sentaurus

Synopsys Sentaurus TCAD version H-2013.03 has been used to obtain the transient response of a FinFET SRAM cell to heavy ion strikes. The 3-D structure for the Tri-Gate SOI FinFET is shown in Fig. 5. It has been constructed with Sentaurus Structure Editor (SDE). Table 1 shows the FinFET parameters used in SDE. They are based on a model

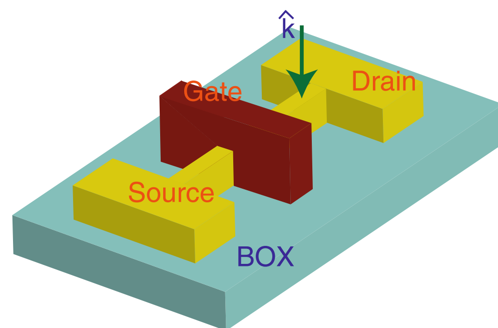


Fig. 5 FinFET structure under an ion strike

Table 1 FinFET's parameters used in this work

Parameter	Value
L(nm)	10
TFIN(nm)	5
HFIN(nm)	12.5
EOT(nm)	0.585
V_{DD} (V)	0.8
N_{SD} (cm^{-3})	3e20
N_{CH} (cm^{-3})	1e15

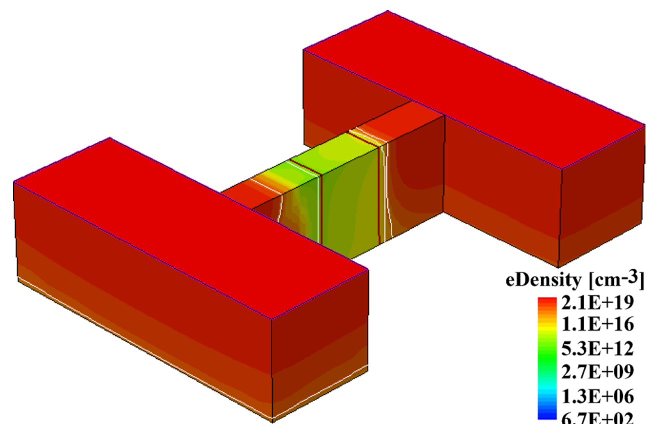
EOT Equivalent Oxide Thickness

card of 10 nm Tri-Gate SOI FinFETs. The value of HFIN given in Table 1 will be named *HFIN reference value*.

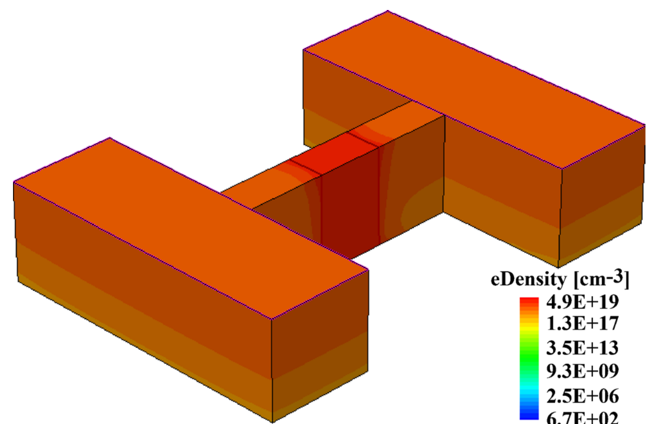
It has been considered a heavy ion strike at the drain terminal of transistor *Mn2* (See Figs. 3 and 5) with a normal incidence angle [7, 14, 17], which is referred as $\hat{k}$ direction strike (See Fig. 5). When a heavy ion strikes the fin with a normal incidence angle, it strikes at the top of the fin and crosses vertically the drain body. The *Linear Energy Transfer* (LET), the ion range depth, and the profile lateral radius values are the input parameters to the heavy ion model for TCAD transient simulation. LET as a function of ion range depth through different layers has been considered. The profile lateral radius is determined by the radial dose model used in [5]. The spatial charge distribution of the ion track was characterized with a Gaussian distribution function [5].

3.1.3 Transient Response using 3-D TCAD

EHPs are generated in the silicon fin when a heavy ion strikes at the drain terminal of transistor *Mn2*. It has been considered a normal incidence angle (See Figs. 3 and 5). Electrons are collected at the drain terminal of transistor *Mn2* due to the higher electric field of the drain-body junction (node *B* in Fig. 3 stores a logic '1'). Thus, the electron density in the silicon fin changes due to the heavy ion strike. Figure 6a shows the 3-D FinFET electron density profile before a strike. A heavy ion with LET=0.9 $MeV-cm^2/mg$ is used. When a heavy ion strike occurs, the electron concentration in the silicon fin considerably increases as shown in Fig. 6b. The excess of electrons in the silicon fin is then collected at the drain terminal of the FinFET transistor. For this case, the collected charge (Q_{coll}) is higher than threshold value Q_{crit}, thus a bit flip occurs in the SRAM cell.



(a) Electron density before strike



(b) Electron density after strike.

Fig. 6 Electron density profile before and after strike. Ion LET=0.9 $MeV-cm^{2/mg}$. For this LET value a bit-flip occurs in the SRAM cell

3.2 Impact of Increasing HFIN on Soft Error Sensitivity

EHPs generation depends on the LET of the heavy ion and the ion range depth into the material. As fin height increases the heavy ion range depth into the silicon fin increases. Because of this, more EHPs are generated within the fin, and as a consequence more charge is collected. This makes the SRAM more sensitive to soft errors. This is illustrated in Fig. 7 for a heavy ion strike with LET=0.3 $MeV-cm^2/mg$. This LET value does not cause a bit flip in the SRAM cell for nominal HFIN value (HFIN=12.5 nm). It is observed that Q_{coll} increases (curve in blue) as HFIN increases.

Nevertheless, not only Q_{coll} increases as HFIN increases but also Q_{crit} does. As mentioned before, Q_{crit} is the threshold collected charge value to a bit flip occurs. Q_{crit} depends on the capacitance at the drain terminal of transistor *Mn2* (node *B*). The value of this capacitance depends on the transistor size. According to Eq. 1, W_{eff} increases as HFIN increases. Because of this, the capacitance raises HFIN increases, and as a consequence Q_{crit} increases. This behavior is illustrated in Fig. 7. It is observed that Q_{crit} increases (curve in black) as HFIN increases.

Even though both Q_{crit} and Q_{coll} increases as HFIN increases, the rate of change of Q_{coll} as HFIN increases is higher than the rate of change of Q_{crit}. From Fig. 7,

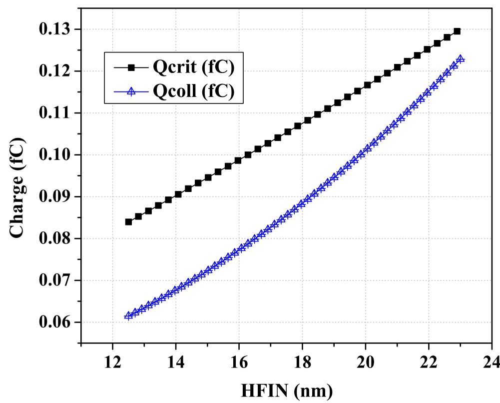


Fig. 7 Q_{crit} and Q_{coll} as a function of HFIN. Heavy Ion LET=0.3 $MeV - cm^2/mg$. For this LET value a bit flip does not occur in the SRAM cell for HFIN nominal value

for HFIN=23 nm Q_{coll} increases 2X with respect to HFIN nominal value while Q_{crit} increases 1.4X. This behavior suggests that heavy ions with low LET values that do not produce a bit flip for nominal HFIN, may cause a bit flip for higher values of HFIN in spite of Q_{crit} increment, making the SRAM cell more sensitive to soft errors.

In this work, the sensitivity to soft errors of a FinFET-based SRAM cell is analyzed based on the *linear energy transfer threshold* (LET_{TH}), which is the minimum LET to cause a SEU. Figure 8 plots the threshold LET (LET_{TH}) as a function of HFIN for the SRAM cell. It can be observed that LET_{TH} decreases as HFIN increases. This shows that FinFET-based SRAM cells becomes more sensitive to soft errors for higher values of HFIN.

3.3 Influence of Process Variations

Analysis of Variance (ANOVA) [9] has been used to quantify the impact of each parameter on Q_{crit} and Q_{coll}. TCAD simulations of a FinFET SRAM cell have been implemented with *Design of Experiments* (DOE) [12]. Full Factorial

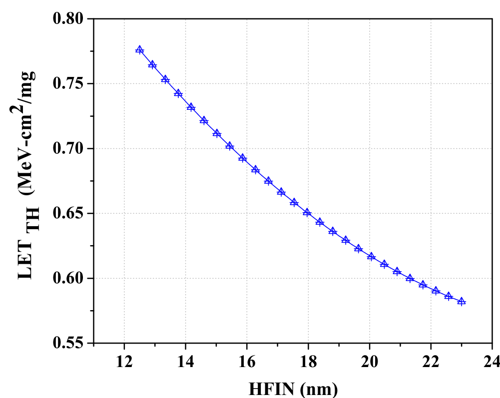


Fig. 8 Threshold LET as a function of HFIN

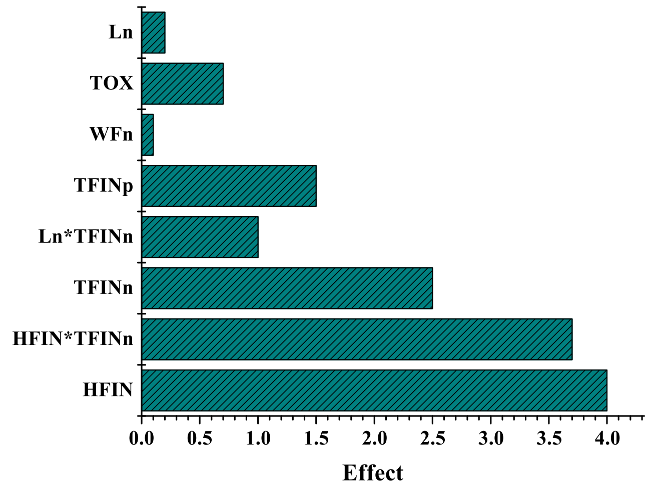


Fig. 9 Q_{crit} Pareto Chart of Effects for a heavy strike at normal incidence ($\hat{k}$ direction). Subindex *n* (subindex *p*) states for parameters of transistor Mn2 (Mp2)

design with 3 levels for each parameter has been used. Process parameter variations are approximated to be normally distributed. Thus, Q_{crit} and Q_{coll} are also approximated to have normal distributions. The analysis has been performed for HFIN reference value (See Table 1). ANOVA analysis allows to quantify statistically the effect of process parameters on Q_{crit} and Q_{coll} as well as their interactions. *Effect* represents the relative weight (impact) of an independent variable on system response. An interaction refers to the impact of a joint behavior of two or more parameters on Q_{crit} and Q_{coll}. Thus, from ANOVA analysis, a *Pareto Chart of Effects* of process parameters has been elaborated for a heavy ion strike in $\hat{k}$ direction at the drain terminal of transistor *Mn2* (See Fig. 3).

Figure 9 plots a *Pareto Chart of Effects* for Q_{crit}. The statistically effect size of each parameter and their interactions are shown. Only those process parameters with a

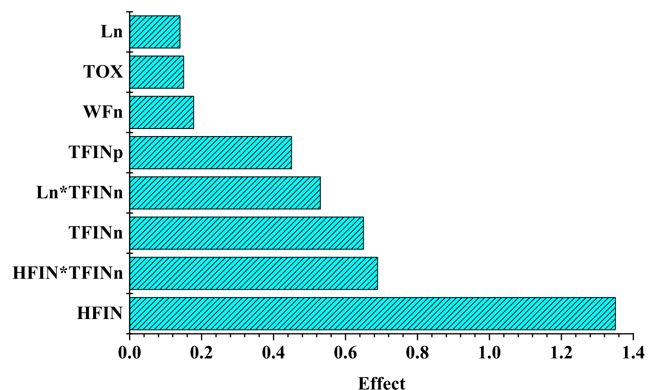


Fig. 10 Q_{coll} Pareto Chart of Effects for a heavy strike at normal incidence ($\hat{k}$ direction). Subindex *n* (subindex *p*) states for parameters of transistor Mn2 (Mp2)

Table 2 Impact of process variations on Qcrit

HFIN (nm)	μ_{Qcrit} (C)	σ_{Qcrit} (C)	$3\sigma/\mu$ (Qcrit)
12.5	$8.3e-17$	$3e-18$	0.1
15	$9.4e-17$	$5.1e-18$	0.16
20	$11.6e-17$	$8.8e-18$	0.22
23	$13e-17$	$9.8e-18$	0.23

larger effect on Q_{crit} are shown. Process parameters of transistors Mp2 and Mn2 (See Fig. 3) have a higher effect on Q_{crit} than the other transistors of the cell. It can be observed that HFIN, $TFIN_n$ and their interaction ($HFIN*TFIN_n$) have a major effect on Q_{crit}. This is congruent considering that HFIN and TFIN define the FinFET effective channel width (See Eq. 1) which impacts the capacitance value of node B (See Fig. 3).

Figure 10 plots the *Pareto Chart of Effects* for Q_{coll}. Similarly to Q_{crit}, process parameters of transistors Mp2 and Mn2 (See Fig. 3) have a larger effect on Q_{coll} than the other transistors of the cell. Unlike to Q_{crit}, it is observed that HFIN has a major effect on Q_{coll}. Thus, the amount of Q_{coll} shows an important dependance on HFIN variations. This is congruent considering the normal incidence angle of the heavy ion strike.

Tables 2 and 3 show the mean (μ), standard deviation (σ) and variability ($3\sigma/\mu$) of Q_{crit} and Q_{coll} for different values of HFIN. As mentioned before, Q_{crit} depends on storage node capacitance while Q_{coll} depends on heavy ion LET and strike location ($\hat{k}$ direction in this work). A heavy ion with LET=0.3 $MeV-cm^2/mg$ is considered, which does not cause a bit flip in the SRAM under nominal conditions. It is observed μ_{Qcoll} (σ_{Qcoll}) grows at a larger rate than μ_{Qcrit} (σ_{Qcrit}) as HFIN increases. Q_{coll} presents a higher dispersion as HFIN increases. Therefore, $3\sigma/\mu$ of Q_{coll} is larger than $3\sigma/\mu$ of Q_{crit}.

These results suggest that process variations have a major impact on Q_{coll} and Q_{crit} distributions as HFIN increases. As mentioned before, a heavy ion with LET=0.3 $MeV-cm^2/mg$ does not cause a bit flip in the SRAM cell under nominal process parameters. However, in presence of process variations a bit flip may occur. Since Q_{coll} and Q_{crit} are assumed to behave as normal distributions with 6σ overall variation, an overlap region between both distributions

Table 3 Impact of process variations on Qcoll

HFIN (nm)	μ_{Qcoll} (C)	σ_{Qcoll} (C)	$3\sigma/\mu$ (Qcoll)
12.5	$6.02e-17$	$3.8e-18$	0.19
15	$6.9e-17$	$5.9e-18$	0.26
20	$9.2e-17$	$10e-18$	0.33
23	$11e-17$	$12.5e-18$	0.35

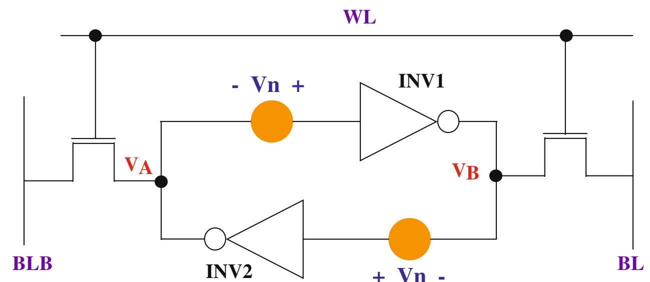


Fig. 11 Static noise margin definition

may appear depending on the values of $\mu_{Qcoll}+3\sigma_{Qcoll}$ and $\mu_{Qcrit}-3\sigma_{Qcrit}$. From the data of Tables 2 and 3, there is not an overlap between the distributions of Q_{coll} and Q_{crit} when HFIN=12.5 nm (HFIN reference value) is the mean value. However, overlap appears when higher values of HFIN are used as the mean value. The overlap increases as the mean values of HFIN increases. As a consequence the probability of a bit flip to occur increases.

4 Impact of Fin Height on SRAM Cell Stability

4.1 Behavior of SRAM Cell Stability

The stability of an SRAM cell is evaluated by the Static Noise Margin (SNM) [15]. The SNM of the SRAM gives an indication of maximum spurious noise that the bit cell can tolerate while still maintaining a reliable operation. The SNM of the SRAM cell is defined as the maximum amount of noise voltage that can be tolerated at the inputs of the crossed coupled inverters while the cell retains its data [15]. The DC sources of noise can be modeled as voltage sources V_n connected in the feedback path as shown in Fig. 11. The polarity of the noise sources is chosen to worse at the same time the voltage levels at both 'true' and 'complement' nodes. The worst-case implies a state of the system that would become unstable with the minimum noise. Thus,

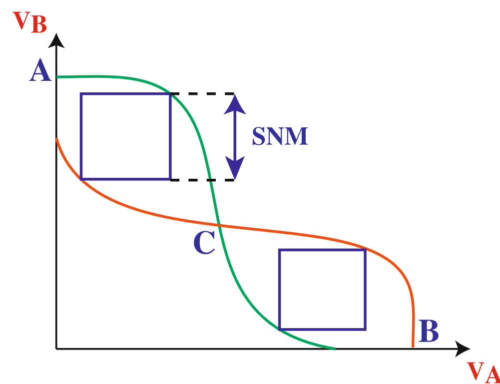


Fig. 12 Butterfly curve

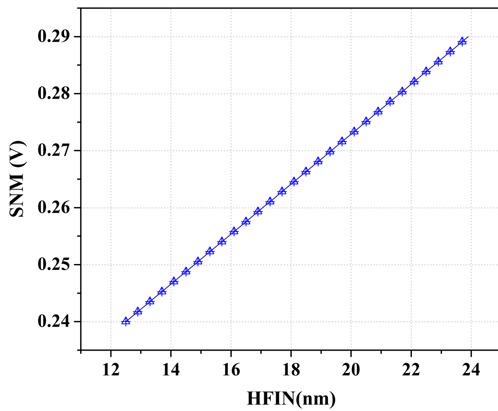


Fig. 13 SNM as a function of HFIN

the minimum value of V_n for which the cell flips or gets disturbed is the minimum noise margin that the bit-cell can tolerate.

The SNM can be obtained by plotting the Voltage Transfer Curves (VTC) of inverters 1 and 2 (See Fig. 11) superimposed on each other. This is depicted in Fig. 12. The transfer curves intersect at three points: A, B and C (”butterfly curve”). Point C has a very large gain and is a metastable point. Therefore, the system has two stable states: one for $V_A = 0$ and $V_B = 1$, and a second for $V_A = 1$ and $V_B = 0$.

The SNM is obtained from the maximum squares that can be inscribed in the wings of the butterfly curve. If the two inverters of the SRAM cell are not identical, the butterfly curve is non-symmetrical, and in this situation, the SNM is given by the smaller of the two maximum squares that can be inscribed in the wings of the butterfly. The SNM of the FinFET-SRAM cell has been computed by simulations in HSPICE version H-2013.03 (BSIM CMG is supported). A model card for 10 nm Tri-Gate SOI FinFET has been used.

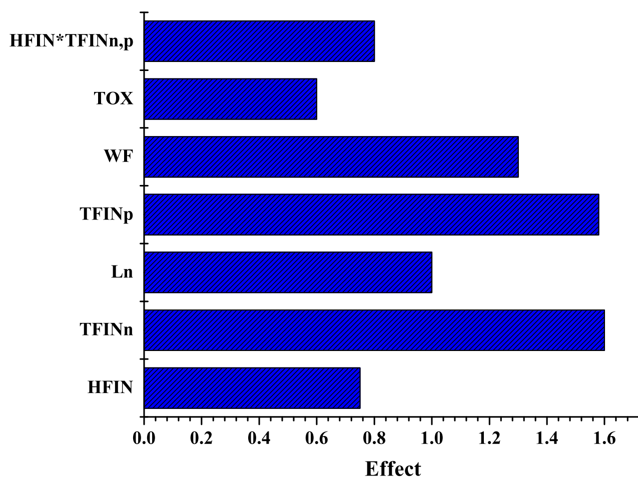


Fig. 14 Pareto Chart of Effects for SRAM SNM. Subindex *n* (subindex *p*) states for parameters of transistor Mn2 (Mp2)

Table 4 Impact of process variations on SNM

HFIN (nm)	μ_{SNM} (mV)	σ_{SNM} (mV)	$3\sigma/\mu$
12.5	238	14	0.17
23	290	15	0.15

4.2 Impact of Increasing HFIN on SRAM Cell Stability

The impact of increasing HFIN on SNM is analyzed. Figure 13 shows the SNM of the FinFET SRAM cell as a function of HFIN. It can be observed that SNM increases as HFIN increases. For HFIN=23 nm, the SNM improves 20 % with respect to HFIN reference value (HFIN=12.5 nm). This result indicates that the stability of the SRAM cell improves as HFIN increases.

4.3 Influence of Process Variations

SNM has been approximated with a normal distribution. *Analysis of Variance* (ANOVA) and *Design of Experiments* (DOE) is used to analyze the impact of process variations on SNM of the SRAM cell. Figure 14 shows the *Pareto Chart of Effects* of SNM. It can observed that opposite to Q_{coll} behavior, HFIN is not the parameter with major effect on SNM, but the SNM variation is mainly affected by TFIN and WF variations.

Table 4 shows μ_{SNM}, σ_{SNM} and $3\sigma/\mu$ values for SNM probability distribution considering HFIN=12.5 nm and HFIN=23 nm. It can be observed that HFIN has a main impact only on μ_{SNM} and not on σ_{SNM} (also observed in the Pareto Chart of Effects - Fig. 14) and as consequence variability of SNM decreases as HFIN increases. These results indicate that increasing HFIN not only improves SNM mean value but also reduce SNM variability.

5 Conclusion

The impact of fin height (HFIN) of FinFET transistors on soft error sensitivity and SRAM cell stability has been analyzed. 3-D TCAD Sentaurus simulations have been used to analyze the charge collection mechanism of an SRAM cell due to a heavy ion strike while Mix-Mode Hspice-TCAD simulations have been used to quantify the Static Noise Margin (SNM) of an SRAM cell. It has been shown that increasing HFIN makes the SRAM cell more sensitive to soft errors. It has been found that both, collected charge (Q_{coll}) and critical charge (Q_{crit}), increase as HFIN increases. However, the rate of change of Q_{coll} is higher than the rate of change of Q_{crit}. Because of this, heavy ions with low LET values may cause a bit flip for higher

values of HFIN in spite of Q_{crit} increment. This behavior reflects on the threshold LET (LET_{TH}). It has been shown that LET_{TH} degrades as HFIN increases. In addition, the impact of process variations on SRAM sensitivity to soft errors has been also analyzed. *Analysis of Variance* (ANOVA) and *Design of Experiments* (DOE) have been used to quantify the impact of process parameters on Q_{coll} and Q_{crit}. A bit flip may occur in the presence of process variations in spite does not occur at nominal values of the process parameters. It has been found that increasing HFIN, the SNM increases improving SRAM stability. Furthermore, increasing HFIN improves SNM mean value and reduce its variability. This suggests that the optimum fin height value of FinFET transistor depends on the best tradeoff between SRAM cell stability and sensitivity to soft errors according to the application.

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