Test Technology Newsletter

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*The Newsletter of the Test Technology Technical Council
of the IEEE Computer Society*

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PAST TTTC EVENTS

The 19th Design Automation & Test in Europe Conference and Exhibition – DATE 2016
14–18 March, 2016, ICC, Dresden, Germany
http://www.date-conference.com

DATE is the major international event for design and engineering of Systems-on-Chip, Systems-on-Board and Embedded Systems Software and states a unique networking opportunity, bringing together designers and design automation users, researchers and vendors, as well as specialists in hardware and software design, test and manufacturing of electronic circuits and systems.

DATE 2016 will take place from 14 to 18 March, 2016, at the International Congress Center Dresden, Germany. It is located at the banks of the river Elbe at walking distance from the city centre and provides state-of-the-art conference facilities. Dresden is a modern and vibrant city with short distances and a cutting-edge technology and economy sector. It is a leading semiconductor site in Europe, concentrating expertise on research, development and manufacturing of leading-edge technologies which drive semiconductor industry to the top. Major players are e.g. GLOBALFOUNDRIES, Infineon, and the Technical University, which is part of the German Excellence Initiative. Silicon Saxony is a registered industry association of 300 companies in the microelectronics and related sectors in Saxony, Germany, with around 20,000 employees. It therefore states an excellent venue for DATE 2016.

2016 IEEE VLSI Test Symposium
25–27 April, 2016, Las Vegas, Nevada, USA
http://tttc-vts.org/public_html/new/2016/

The IEEE VLSI Test Symposium (VTS) explores emerging trends and novel concepts in testing, debug and repair of microelectronic circuits and systems. The VTS Program Committee invites original, unpublished paper submissions for VTS 2016. Paper submissions should be complete manuscripts, up to six pages (inclusive of figures, tables, and bibliography) in a standard IEEE two-column format; papers exceeding the page limit will be returned without review. Authors should clearly explain the significance of the work, highlight novel features, and describe its current status. On the title page, please include: author name(s) and affiliation(s), and the mailing address, phone number, and e-mail address of the contact author. A 50-word abstract and five keywords identifying the topic area are also required.

UPCOMING TTTC EVENTS

2016 IEEE International Symposium on On-Line Testing and Robust System Design
4–6 July, 2016, Sant Feliu de Guixols, Catalunya, SPAIN
http://tima.imag.fr/conferences/iolts

Issues related to On-line testing techniques, and more generally to design for robustness, are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective design for robustness techniques. These needs have increased dramatically with the introduction of nanometer technologies, which impact adversely noise margins; process, voltage and temperature variations; aging and wear-out; soft error and EMI sensitivity; power density and heating; and make mandatory the use of design for robustness techniques for extending, yield, reliability, and lifetime of modern SoCs. Design for reliability becomes also mandatory for reducing power dissipation, as voltage reduction, often used to reduce power, strongly affects reliability by reducing noise margins and thus the sensitivity to soft-errors and EMI, and by increasing circuit delays and thus the severity of timing faults. There is also a strong relation between Design for Reliability and Design for Security, as security attacks are often fault-based.

Springer

The International Symposium on On-Line Testing and Robust System Design (IOLTS), is an established forum for presenting novel ideas and experimental data on these areas. The Symposium is sponsored by the IEEE Council on Electronic Design Automation (CEDA) and the 2016 edition is organized by the IEEE Computer Society Test Technology Technical Council, the University of Athens, and the TIMA Laboratory.

2016 1st IEEE Federative Event on Design for Robustness (FEDfRo)

4–6 July, 2016, Sant Feliu de Guixols, Catalunya, SPAIN
http://tima.imag.fr/conferences/fedfro/fedfro16/

Nanometer scaling and the related aggressive reduction of device geometries steadily worsens noise margins; process, voltage and temperature variations; aging and wear-out; soft error and EMI sensitivity; power density and heating; and make mandatory the use of efficient techniques for improving yield and reliability, extending lifespan, and reducing power dissipation of modern SoCs. Additionally, the rapidly increasing complexity of modern SoCs further aggravates these issues, and makes it extremely difficult to guarantee that the design of these chips meet their specifications.

Furthermore, the pervasiveness of electronic systems in modern societies, and their ubiquitous implication in all aspects of our everyday lives, drastically raises the requirements to protect modern electronic systems against all these threats, as well as versus those induced by intentional attacks against their security.

These trends have made mandatory the development of efficient Design for Robustness approaches for mitigating these pluralities of threats. However, as DfX techniques are proliferating (Design for Test, Design for Debug, Design for Yield, Design for Reliability, Design for Low-Power, Design for Security, Design for Verification, …), it becomes mandatory to address these issues holistically, in order to moderate their impact on area, power, and/or performance, and increase their global efficiency. There is therefore a related need for an international consolidated forum bringing together specialists from all these domains to enhance interactions and cross-fertilization. The IEEE Federative Event on Design for Robustness (FEDfRo) was initiated to meet this goal.

The 25th IEEE Asian Test Symposium

21–24 November, 2016, Hiroshima, JAPAN
http://aries3a.cse.kyutech.ac.jp/~ats16/

The Asian Test Symposium (ATS) provides an international forum for engineers and researchers from all countries of the world, especially from Asia, to present and discuss various aspects of device, board and system testing with design, manufacturing and field considerations in mind.

The ATS'16 Program Committee invites original, unpublished paper submissions for ATS'16. Paper submissions should be complete manuscripts, up to six pages (including figures, tables, and bibliography) in a standard IEEE two-column format; papers exceeding the page limit will be returned without review. Authors should clearly explain the significance of the work, highlight novel features, and describe its current status. On the title page, please include: author name(s) and affiliation(s), and the mailing address, phone number, fax number, and e-mail address of the contact author. An abstract of 50 words or less and 5–10 keywords are also required. All submissions are to be made electronically through the ATS'16 website. Detailed instructions for submissions are to be found at the ATS'16 website. Electronic submissions in PDF files are strongly recommended. A submission will be considered as evidence that, upon acceptance, the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The registration of at least one author is required for publication.

NEWSLETTER EDITOR'S INVITATION

I would appreciate input and suggestions about the newsletter from the test community. Please forward your ideas, contributions, and information on awards, conferences, and workshops to Theocharis (Theo) Theocharides, Department of Electrical and Computer Engineering, University of Cyprus, 75 Kallipoleos Avenue, PO Box 20537, Nicosia, 1678, CYPRUS; ttheocharides@ucy.ac.cy.

Theo Theocharides
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CONTRIBUTIONS TO THIS NEWSLETTER:

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