Chapter 1. An Overview of Built-In Self-Test

1. Excluding the circuit under test, what are the four basic components of BIST and what function does each component perform?

   1) The test pattern generator (TPG) produces the test patterns to be applied to the circuit under test.

   2) The output response analyzer compacts the output responses of the circuit under test into some type of *pass/fail* indication.

   3) The test controller controls initialization of the TPG, ORA, and circuit under test. The test controller also controls the length of the BIST sequence.

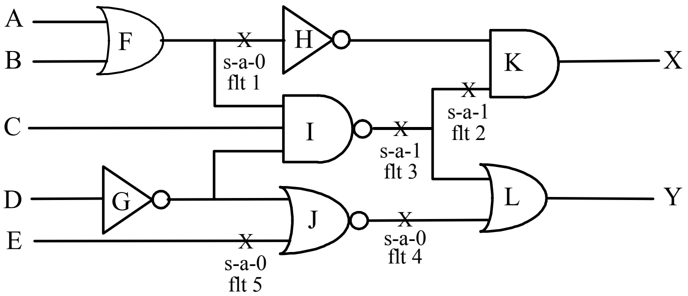
   4) Input isolation circuitry prevents unknown system data from entering the BIST circuitry, particularly the circuit under test and the ORA, during the BIST sequence.

2. Which two BIST components are necessary for system-level testing and why?

   The test controller and the input isolation circuitry are necessary for system-level testing to obtain reproducible results from one execution of the BIST sequence to the next. These components are not essential during manufacture testing since these functions can be performed by external test equipment.

Chapter 2. Fault Models, Detection, and Simulation

1. Given the following gate-level circuit diagram:



a. Does the circuit contain reconvergent fanout?
Yes, in two places (gate F through gates H and I to gate K, and gate G through gates I and J to gate L)

b. How many faults sites are in the circuits? 20 = 13 gate inputs + 7 gate outputs

c. What is the total number of uncollapsed single stuck-at gate-level faults?
40 = 2×13 gate inputs + 2×7 gate outputs

d. What is the total number of collapsed single stuck-at gate-level faults?
21 = 13 gate inputs + 2×2 primary outputs + 2×3 fanout stems – 2 inverters

e. What is the total number of faulty circuits considered in the multiple stuck-at gate-level fault model? 3^{20}-1 (the 1 being the fault-free circuit)

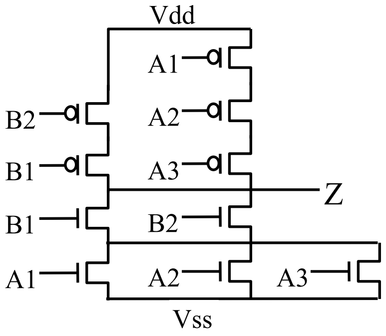
f. Give the complete set of collapsed single stuck-at gate-level faults.

Gate	**Signal**	**I/O**	**Stuck-at**	**Gate**	**Signal**	**I/O**	**Stuck-at**	**Gate**	**Signal**	**I/O**	**Stuck-at**
F	A	In	S-a-0	I	C	In	S-a-1	K	H	In	S-a-1
F	B	In	S-a-0	I	F	In	S-a-1	K	I	In	S-a-1
F	F	Out	S-a-0	I	G	In	S-a-1	K	K	Out	S-a-1
F	F	Out	S-a-1	I	I	Out	S-a-1	K	K	Out	S-a-0
G	G	Out	S-a-0	I	I	Out	S-a-0	L	I	In	S-a-0
G	G	Out	S-a-1	J	E	In	S-a-0	L	J	In	S-a-0
J	G	In	S-a-0	L	L	Out	S-a-0	L	L	Out	S-a-1

g. For each of the five single stuck-at gate-level faults shown in the circuit, use path sensitization to determine whether the fault is detectable or not. If the fault is detectable, give a test pattern (indicating input ordering) that will detect the fault and indicate the output(s) at which the fault will be detected.

Fault	**Detectable?**	**Test vector (ABCDE)**	**Output(s)**
1	Yes	1X0XX	K
2	No, a conflict exists at output of gate F		
3	Yes	1X10X	L
4	No, a conflict exists at output of gate G		
5	No, a conflict exists at output of gate G		

2. Given the following transistor-level circuit diagram:



   a. How many fault sites are in the circuit?

      10 = 5 NFETs + 5 PFETs

   b. What is the total number of uncollapsed single stuck-at transistor-level faults?

      20 = 2×10 transistors

   c. What is the total number of collapsed single stuck-at transistor-level faults?

      14 = 2×10 transistors – 5 series transistors + 2 groups of series transistors – 5 parallel transistors + 2 groups of parallel transistors

3. What type of transistor-level faults are detected by I_{DDQ} testing?
   transistor stuck-on faults

4. Assume that a circuit has 400 faults and that for a given set of test vectors, 350 faults are detected, 50 faults are not detected and 30 faults are potentially detected. Calculate the fault coverage.

$$FC = \frac{\#\text{detected faults} + 1/2 \times \#\text{ potentially detected faults}}{\#\text{ total faults}} = \frac{350+15}{400} = 87.5\%$$

Chapter 3. Design for Testability

1. Assume a sequential circuit with 100 flip-flops plus 1000 additional logic gates, 20 primary inputs, and 15 primary outputs.
   a. Determine the area overhead in terms of gates for a full scan design implementation assuming a multiplexer is 3 gates and a flip-flop is 9 gates.

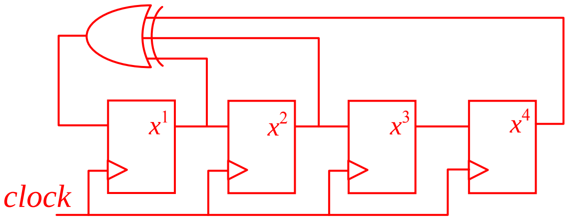
      Total gates w/o DFT = 100 FFs × 9 gates/FF + 1000 gates = 1900 gates
      Total gates w/DFT = 1900 gates + 100 FFs × 3 gates/scanFF = 2200 gates
      Area overhead = 2200 gates / 1900 gates = 115.8% (usually reported as 15.8%)

   b. Determine the number of clock cycles needed for scan testing if the combinational logic portion of the circuit requires 50 test vectors.

      $N_{CC} = 50\ TVs \times (100 \text{ FFs} + 1) + 100 \text{ FFs} + 8 = 5{,}158$ clock cycles

Chapter 4. Test Pattern Generation

1. Assume the polynomial $P(x)=x^4+x^2+x+1$:
   a. Design an external feedback LSFR with characteristic polynomial $P(x)$.



   b. Starting this LFSR in the all 1s state, determine the sequence produced.
   1111→1111

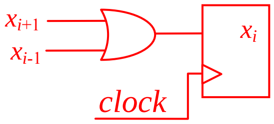
   c. Is this a maximal length LFSR?
   No, it locks up in the all 1s state

   d. Is the characteristic polynomial primitive?
   No

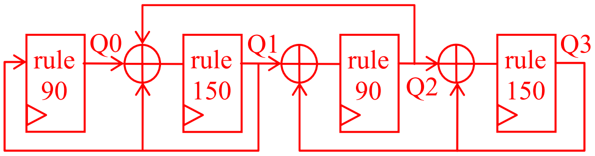
2. Design a register bit for CA rule 175 and draw the logic diagram labeling all I/O?

Rule 175	7	6	5	4	3	2	1	0
$x_{i-1}(t)\ x_i(t)\ x_{i+1}(t)$	111	110	101	100	011	010	001	000
$x_i(t+1)$	1	0	1	0	1	1	1	1
value = 175	2^7		2^5		2^3	2^2	2^1	2^0

$$x_i(t+1) = x_{i-1}(t) + x_{i+1}(t)$$



3. Assume a 4-bit CA register with null boundary conditions that uses alternating rules of 90 and 150:
   a. Draw a gate and flip-flop level diagram of the complete register.

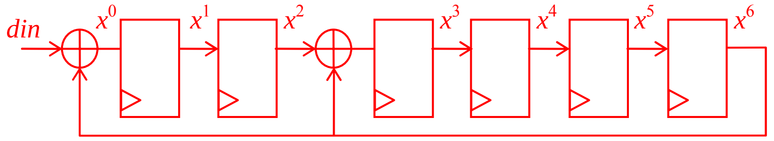


   b. Determine the sequence of test patterns produced by this register once it has been preset to the all 1s state.

Q0	Q1	Q2	Q3
1	1	1	1
1	1	0	0
1	0	1	0
0	0	0	1
0	0	1	1
0	1	1	0
1	0	1	1
0	0	1	0
0	1	0	1
1	1	0	1
1	0	0	1
0	1	1	1
1	0	0	0
0	1	0	0
1	1	1	0
1	1	1	1

Chapter 5. Output Response Analysis

1. For an internal feedback Signature Analysis Register with characteristic polynomial $P(x)=x^6+x^2+1$:
   a. Draw a logic diagram for the complete register.



   b. Determine the resultant signature that would be obtained for the following serial sequence of output responses produced by a known good CUT assuming the SAR is initialized to the all 0s state. Give the binary value of the resultant signature as it would be contained in the SAR in your logic diagram above.

101001010010 ← *time*

$D(x)= x^{10}+x^7+x^5+x^2+1$

$$\begin{array}{r|l}
 & x^4+x+1 \\ \hline
x^6+x^2+1 & x^{10}+x^7\ +x^5\quad +x^2\ +1 \\
 & x^{10}\quad +x^6\ +x^4 \\ \cline{2-2}
 & \quad x^7+x^6+x^5+x^4+x^2+1 \\
 & \quad x^7\qquad\quad +x^4\quad +x \\ \cline{2-2}
 & \qquad x^6+x^5+x^2+x+1 \\
 & \qquad x^6\qquad +x^2\quad +1 \\ \cline{2-2}
 & \qquad\quad x^5+x
\end{array}$$

$x^5+x \Rightarrow$ 010001 for order shown in figure above

   c. Give the error polynomial assuming the following serial sequence of output responses produced by a faulty CUT. Would this error polynomial lead to signature aliasing?

011001110010 ← *time*

$E(x)= x^6+x$

$E(x)$ is not a multiple of $P(x)$ and, therefore, signature aliasing will not occur