A *JSSC* Classic Paper:

The Simple Model of CMOS Drain Current

In a recent update of the Web list of frequently cited *JSSC* articles, an April 1990 paper by Takayasu Sakurai and A. Richard Newton on "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas" joined the list of articles cited more than 100 times according to the annual *Journal Citation Reports* published by Thomson ISI. At the time the paper was written, Sakurai had just taken a break from a seven-year career working on memories at Toshiba to come to the University of California, Berkeley, as a visiting scholar and worked with Richard Newton, the dean of Berkeley's Electrical Engineering Department. Writing now from the Center for Collaborative Research and the Institute of Industrial Science at the University of Tokyo, Sakurai summarizes the inspiration and impact of this paper.

Alpha Power-Law MOS Model

This paper contains the first proposal of the alpha power-law MOS model, which is a simple yet practical drain-current model for short-channel MOSFETs. The model has been widely used in circuit designs and circuit behavior modeling. Mathematically, it is so simple that it can be used not only for simulations (1) but also for analytical treatments of circuit behavior. Expressions for power consumption, delay, logical threshold, and other quantities are derived using the model in the paper.

The basic concept is that the drain current of short-channel MOSFETs is proportional to $(V_{GS} - V_{TH})^{\alpha}$, where V_{GS} is the gate-to-source voltage, V_{TH} is the threshold voltage, and alpha is a carrier velocity saturation index. It is a natural extension of the historical Shockley model since it coincides with the Shockley model when alpha is set to 2. For the recent short-channel MOSFETs, alpha is typically around 1.3. Before the alpha power-law MOS model, there were many MOS models but they were far more complicated, and manipulating the models analytically did not give fruitful results for circuit designers.

Analytical expressions for the serially connected MOSFET structure, which is the basic structure found in basic NAND and NOR gates, also have been analyzed and delay expressions for the structure have been derived using the model (2). Suppose that n transistors are connected in series and discharge a load capacitor. The delay ratio of the circuit compared with a single transistor discharging the same load capacitor is reduced as alpha decreases. This means that serial connection in shorter channel devices is not as bad as in longer channel devices. Circuit behavior of more complex circuits, such as SRAM cells and sense amplifiers, also has been analyzed by the model (3).

The conception of the model occurred when I was looking at the measured drain current curve of a 1.2-µm MOSFET. I noticed that the I-V curve did not show the quadratic dependence as was taught in textbooks. Instead, it showed that the dependence was close to linear. What simple mathematical expression could represent both quadratic and linear dependence? The simplest would be to use x^{α}. By plotting measured short-channel MOS I-V curves down to a 0.5-µm channel length, the conjecture was shown to be true. The alpha-power function could fit to the measured curves quite well. Why did I use the Greek character α? It was because α is the first Greek character and most of the other Greek characters were taken by other quantities such as β for β ratio and γ for body bias coefficient.

When the model was first introduced, it was purely empirical and mathematical, without physical background. After a while, however, the physical interpretation of the alpha-power dependency was investigated by multiple authors (4, 5) and it was determined that the origin of the alpha-power dependence is based on mobility degradation at high electric fields. Efforts also have been made to connect the exponential dependence of subthreshold current, I_{SUB}, and the alpha-power dependence of on current, I_{ON} as follows, where s signifies subthreshold swing (6):

$$I_{ON} = I_0(S\alpha)^{-\alpha}(V_{GS} - V_{TH})^{\alpha},\ I_{SUB} = I_0 e^{-\alpha} e^{\frac{V_{GS}-V_{TH}}{S}}$$

In the paper the method to extract alpha from the I-V curves is also discussed. But with each generation of technology advances since 1990, V_{DD} has been decreased, and alpha is now almost fixed at about 1.3. This may be a result of the electric field being almost constant in these devices, which leads to nearly constant carrier velocity saturation.

Since the alpha-power model reproduces the voltage dependence of the drain current of MOSFETs very well, being independent from structures and materials of MOSFETs, it is often used to predict the scaling trend of

VLSIs. Now that sub-volt design is becoming mainstream, the voltage dependence of CMOS gate delay is of great importance. By using the model, the delay is proportional to the following quantity:

$$\text{delay} \propto \frac{V_{DD}}{(V_{DD} - V_{TH})^{\alpha}}$$

This relationship is often used to estimate delay trends for the future and it also is used for circuit designs where the V_{DD} and V_{TH} are varied in time. These variable V_{DD} and V_{TH} designs are getting a mainstream design style to cope with the ever-increasing dynamic and leakage power consumption of LSIs. The body bias effect is important in variable V_{TH} design and the body bias effect of serially connected MOSFETs is also analyzed by the alpha-power model (7). Since the model is very simple and comprehensive, it will continue to be used in estimating behavior of MOSFET circuits.

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A *JSSC* Classic Paper: Sigma-Delta Converters

The 1988 classic paper by Bernhard E. Boser and Bruce A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," joins the Web list of frequently cited articles from the *JSSC* (sscs.org/jssc/top-cites.htm). The list contains *Journal* articles that have been cited more than 100 times according to the recently updated *Scientific Index* published by Thomson ISI. There are only 26 articles on this list out of over 7,000 *JSSC* published articles, making it a *singular* honor to be included.

The December 1988 paper provides a classic and clear explanation of why Nyquist sampling theory alone is insufficient for efficient analog-to-digital converters, beginning with, "The oversampled A/D converter architecture offered a means of exchanging resolution in time for amplitude, in order to avoid the difficulty of implementing complex precision analog circuits."

The article is described in the accompanying article on the IEEE Solid-State Circuit Award to Wooley and has been referenced in the *JSSC*, the *Transactions Circuits and Systems II: Analog and Digital Signal Processing*, the *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems*, and the *IEEE Transaction on Instrumentation and Measurement*.

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