CSV 881: Low-Power Design
Fall 2013

Homework 5 Problems

Assigned 28/10/13, due 30/10/13

Note: Submit solution as hardcopy or by email to Sharat Chandra Varma, Bharti Bldg, Architecture Lab (505), anz088224@cse.iitd.ac.in.

**Problem 1:** A CMOS processor has a rated supply voltage 1.5V and clock frequency 2GHz. Its average power consumption is 100W, which consists of 75W dynamic power and 25W static power. Assume that the delay of a gate in the technology is proportional to VDD/(VDD – Vt), where threshold voltage Vt = 0.5V. A low energy mode uses a lower supply voltage and a reduced frequency clock. Determine the voltage and clock frequency that will minimize the average energy consumption per cycle. Compare the power consumption and energy per cycle for the rated and low energy modes.

**Problem 2:** The alpha-power law is often used to characterize the voltage-delay relationship of digital circuits. See <http://www.ieee.org/organizations/pubs/newsletters/sscs/oct04/jssc.pdf>. Thus, we can express the maximum clock frequency of a circuit as f = K(V – Vth)α/V, where V is the supply voltage, Vth is threshold voltage assumed to be the same for p and n devices, and K and α are constants specific to the circuit and technology. To characterize a circuit, its maximum clock rate is determined at two voltages: (a) V = 2 volts, f = 1.380GHz and (b) V = 1 volt, f = 428MHz. Assuming Vth = 0.35 volt, find a consistent set of values for K and α.

**Problem 3:** The circuit of Problem 2 was originally designed for operation with a 2 volts supply and clock rate of 1.38GHz. To reduce power consumption, consider parallel core designs. What should be the supply voltages for (a) dual core and (b) quad core designs? What are respective power savings? Neglect short circuit power and leakage and assume 10% overhead for each additional core.