



VLSI Design and Test Seminar (ELEC7950-001)

Wireless Engineering Research and Education Center

A Non-Linear Neural Classifier and its Applications in Testing Analog/RF Circuits

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Abstract

In this talk, I will be discussing a machine learning-based test paradigm for mixed-signal/RF circuits. I will first describe an ontogenic neural classifier that learns to separate the nominal from the faulty chip distributions in a low-dimensional space of inexpensive measurements. The key novelty of this classifier is that its topology is not fixed; rather, it adapts dynamically, in order to match the inherent complexity of the separation problem. Thus, it establishes separation hypersurfaces that reciprocate very well even in the presence of complex chip distributions. I will then discuss the construction of guard-bands, which provide a level-of-confidence indication and support a two-tier test method which allows exploration of the trade-off between test quality and test cost. In this method, the majority of chips are accurately classified through inexpensive measurements, while the small fraction of chips for which the decision of the classifier has a low level of confidence is re-tested through traditional specification testing. The ability of the proposed method to drastically reduce the cost of mixed-signal/RF testing without compromising its quality will be demonstrated using two example circuits, a switched-capacitor filter and a UHF receiver front-end. Additionally, its application in analog specification test compaction and its potential for developing a stand-alone analog/RF BIST method will be discussed.

Bio

Yiorgos Makris received the Diploma of Computer Engineering and Informatics from the University of Patras, Greece, in 1995, and the M.S. and Ph.D. degrees in Computer Engineering from the University of California, San Diego, in 1997 and 2001, respectively. He then joined Yale University where he is currently an Associate Professor of Electrical Engineering and Computer Science and leads the Testable and Reliable Architectures (TRELA) Laboratory. His research interests are in the areas of test and reliability of analog, digital, and asynchronous circuits and systems.

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