Analog Functional Testing in Mixed-Signal Systems
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BIST Auburn University
Built-In Self-Test
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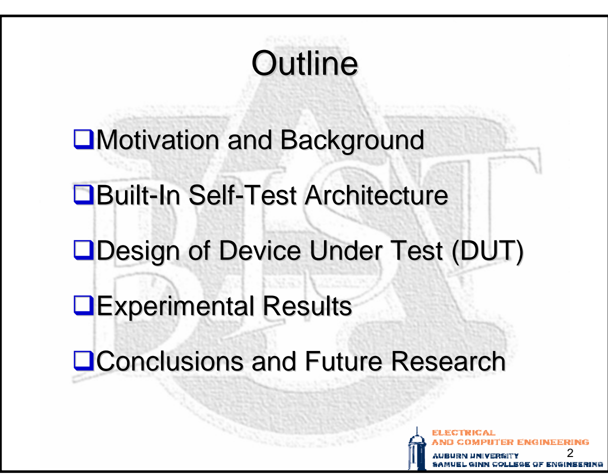

Outline
Motivation and Background
Built-In Self-Test Architecture
Design of Device Under Test (DUT)
Experimental Results
Conclusions and Future Research
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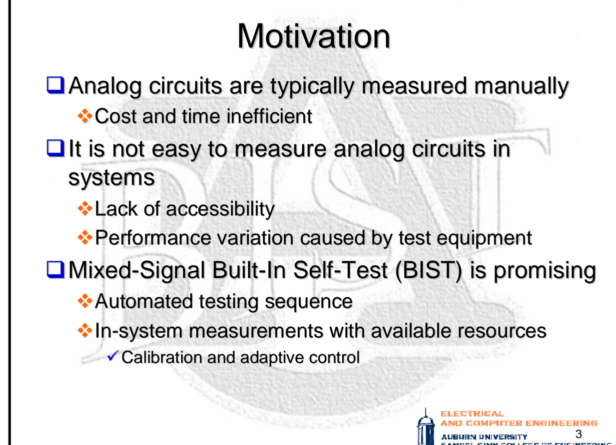

Motivation
Analog circuits are typically measured manually
Cost and time inefficient
It is not easy to measure analog circuits in systems
Lack of accessibility
Performance variation caused by test equipment
Mixed-Signal Built-In Self-Test (BIST) is promising
Automated testing sequence
In-system measurements with available resources
Calibration and adaptive control
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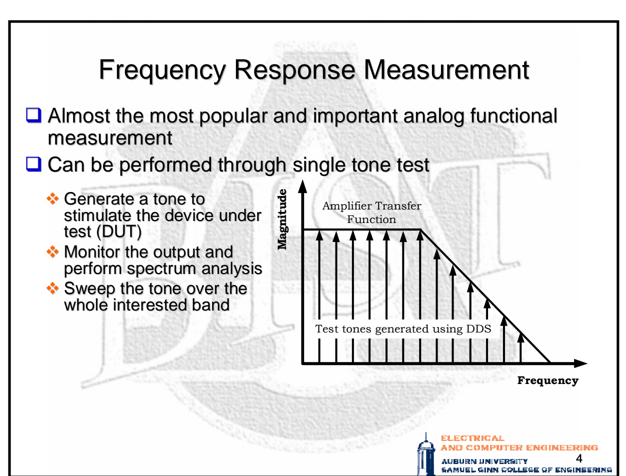

Frequency Response Measurement
Almost the most popular and important analog functional measurement
Can be performed through single tone test
Generate a tone to stimulate the device under test (DUT)
Monitor the output and perform spectrum analysis
Sweep the tone over the whole interested band
Magnitude
Amplifier Transfer Function
Test tones generated using DDS
Frequency
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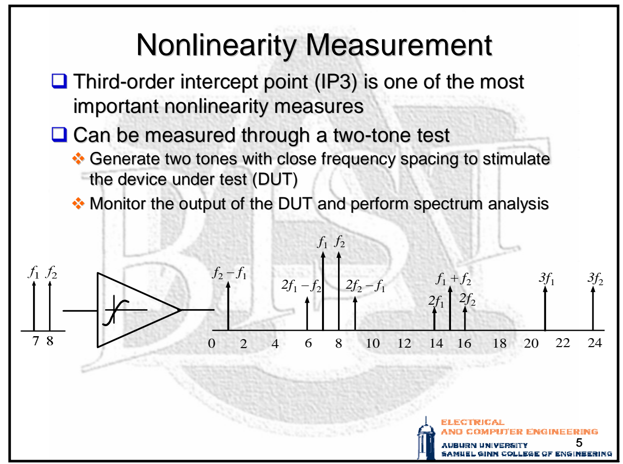
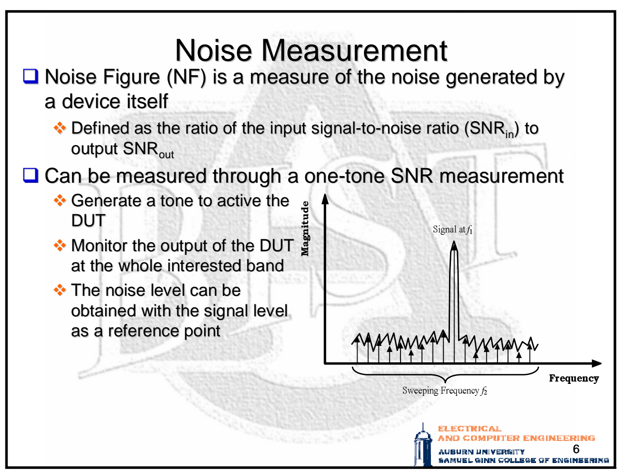


Nonlinearity Measurement
Third-order intercept point (IP3) is one of the most important nonlinearity measures
Can be measured through a two-tone test
Generate two tones with close frequency spacing to stimulate the device under test (DUT)
Monitor the output of the DUT and perform spectrum analysis
f_1 f_2
7 8
$f_2 - f_1$
$2f_1 - f_2$
f_1 f_2
$2f_2 - f_1$
$f_1 + f_2$
$2f_1$
$2f_2$
$3f_1$
$3f_2$
0 2 4 6 8 10 12 14 16 18 20 22 24
5



Noise Measurement
Noise Figure (NF) is a measure of the noise generated by a device itself
Defined as the ratio of the input signal-to-noise ratio (SNR_{in}) to output SNR_{out}
Can be measured through a one-tone SNR measurement
Generate a tone to active the DUT
Monitor the output of the DUT at the whole interested band
The noise level can be obtained with the signal level as a reference point
Magnitude
Signal at f_1
Frequency
Sweeping Frequency f_2
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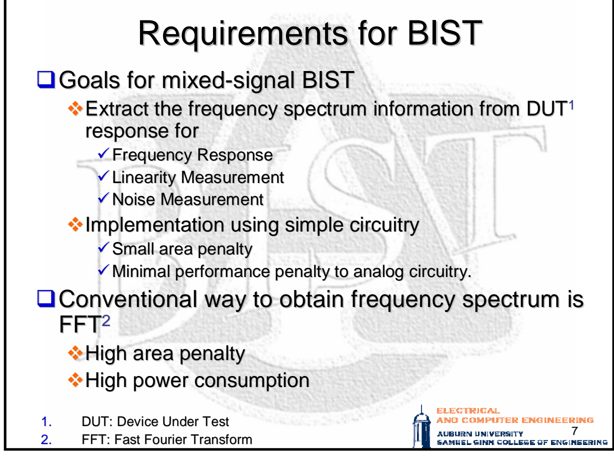

Requirements for BIST
Goals for mixed-signal BIST
Extract the frequency spectrum information from DUT[1] response for
Frequency Response
Linearity Measurement
Noise Measurement
Implementation using simple circuitry
Small area penalty
Minimal performance penalty to analog circuitry.
Conventional way to obtain frequency spectrum is FFT[2]
High area penalty
High power consumption
1. DUT: Device Under Test
2. FFT: Fast Fourier Transform
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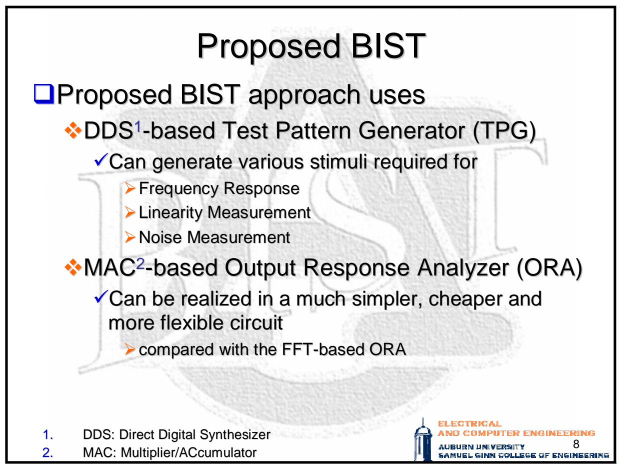

Proposed BIST
Proposed BIST approach uses
DDS[1]-based Test Pattern Generator (TPG)
Can generate various stimuli required for
Frequency Response
Linearity Measurement
Noise Measurement
MAC[2]-based Output Response Analyzer (ORA)
Can be realized in a much simpler, cheaper and more flexible circuit
compared with the FFT-based ORA
1. DDS: Direct Digital Synthesizer
2. MAC: Multiplier/ACcumulator
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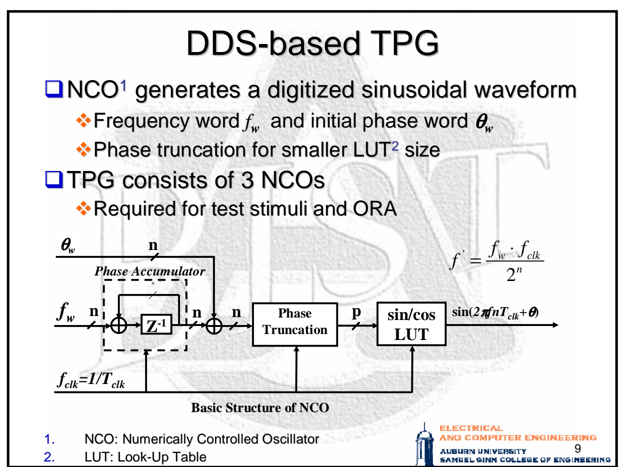
DDS-based TPG
NCO1 generates a digitized sinusoidal waveform
Frequency word fw and initial phase word θw
Phase truncation for smaller LUT2 size
TPG consists of 3 NCOs
Required for test stimuli and ORA
Phase Accumulator
Z-1
Phase Truncation
sin/cos LUT
sin(2πfnTclk+θ)
fclk=1/Tclk
Basic Structure of NCO
1. NCO: Numerically Controlled Oscillator
2. LUT: Look-Up Table
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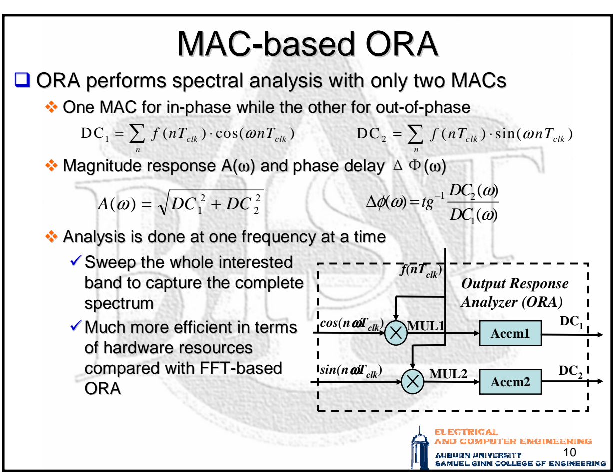
MAC-based ORA
ORA performs spectral analysis with only two MACs
One MAC for in-phase while the other for out-of-phase
Magnitude response A(ω) and phase delay ΔΦ(ω)
Analysis is done at one frequency at a time
Sweep the whole interested band to capture the complete spectrum
Much more efficient in terms of hardware resources compared with FFT-based ORA
Output Response Analyzer (ORA)
MUL1
MUL2
Accm1
Accm2
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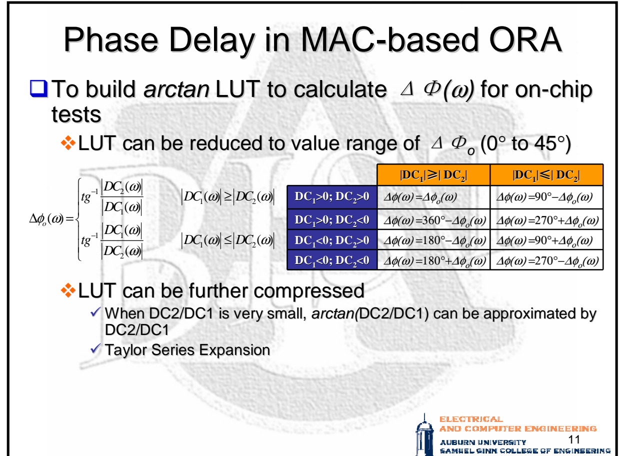
Phase Delay in MAC-based ORA
To build arctan LUT to calculate ΔΦ(ω) for on-chip tests
LUT can be reduced to value range of ΔΦo (0° to 45°)
LUT can be further compressed
When DC2/DC1 is very small, arctan(DC2/DC1) can be approximated by DC2/DC1
Taylor Series Expansion
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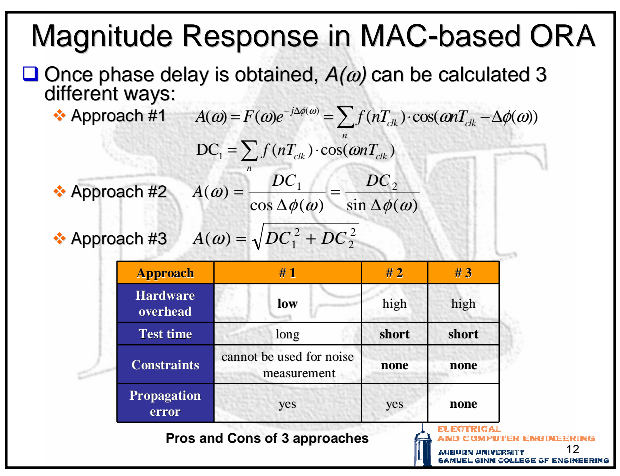
Magnitude Response in MAC-based ORA
Once phase delay is obtained, A(ω) can be calculated 3 different ways:
Approach #1
Approach #2
Approach #3
Approach | # 1 | # 2 | # 3
Hardware overhead | low | high | high
Test time | long | short | short
Constraints | cannot be used for noise measurement | none | none
Propagation error | yes | yes | none
Pros and Cons of 3 approaches
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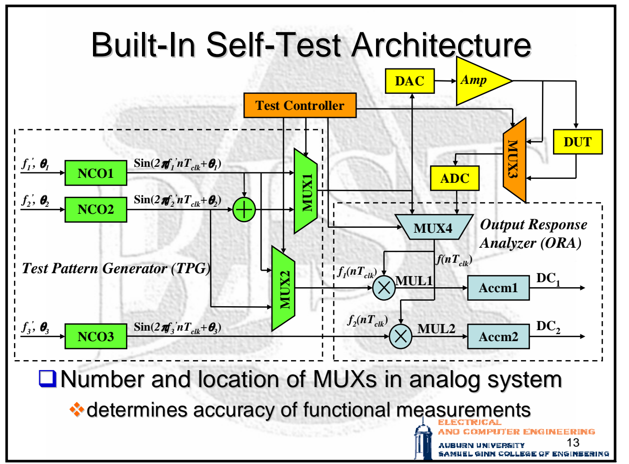
Built-In Self-Test Architecture
DAC
Amp
Test Controller
DUT
NCO1
NCO2
NCO3
MUX1
MUX2
MUX3
MUX4
ADC
Output Response Analyzer (ORA)
Test Pattern Generator (TPG)
MUL1
MUL2
Accm1
Accm2
Number and location of MUXs in analog system
determines accuracy of functional measurements
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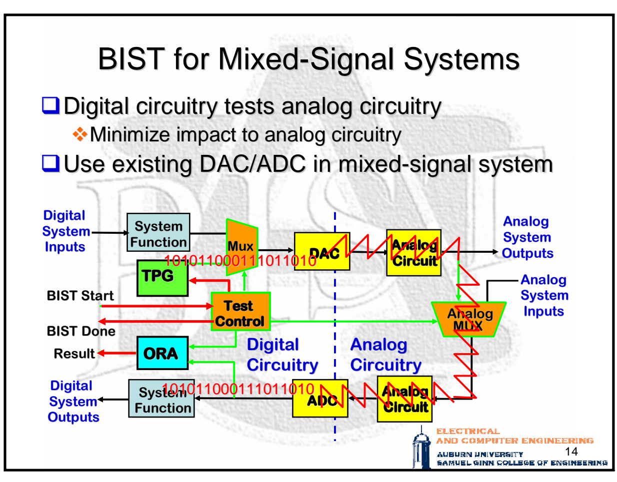
BIST for Mixed-Signal Systems
Digital circuitry tests analog circuitry
Minimize impact to analog circuitry
Use existing DAC/ADC in mixed-signal system
Digital System Inputs
System Function
Mux
DAC
Analog Circuit
Analog System Outputs
TPG
BIST Start
Test Control
Analog MUX
Analog System Inputs
BIST Done
Result
ORA
Digital Circuitry
Analog Circuitry
Digital System Outputs
System Function
ADC
Analog Circuit
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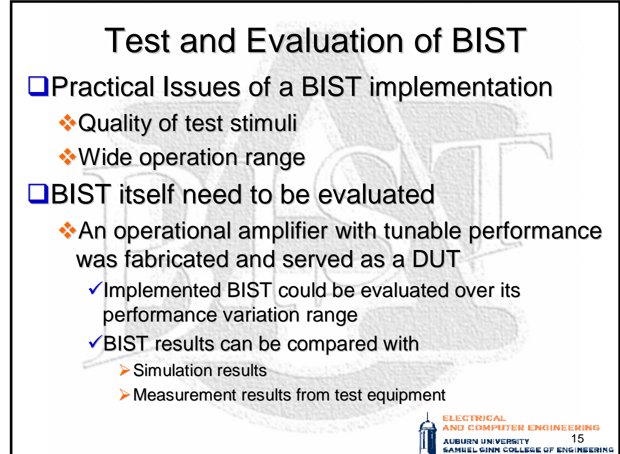
Test and Evaluation of BIST
Practical Issues of a BIST implementation
Quality of test stimuli
Wide operation range
BIST itself need to be evaluated
An operational amplifier with tunable performance was fabricated and served as a DUT
Implemented BIST could be evaluated over its performance variation range
BIST results can be compared with
Simulation results
Measurement results from test equipment
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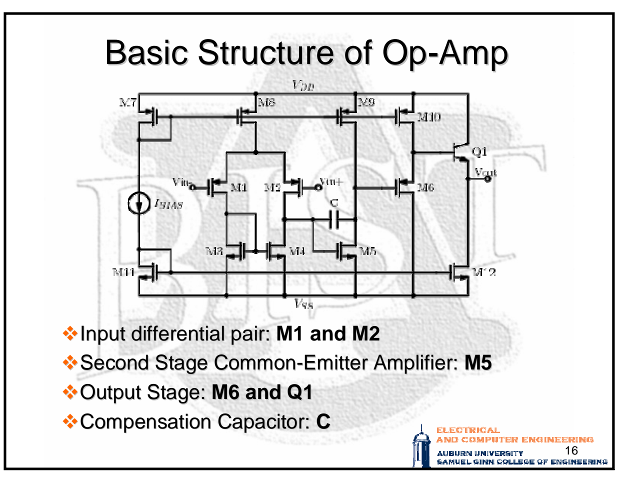
Basic Structure of Op-Amp
M7
M8
M9
M10
Q1
M1
M2
M6
C
M3
M4
M5
M11
Input differential pair: M1 and M2
Second Stage Common-Emitter Amplifier: M5
Output Stage: M6 and Q1
Compensation Capacitor: C
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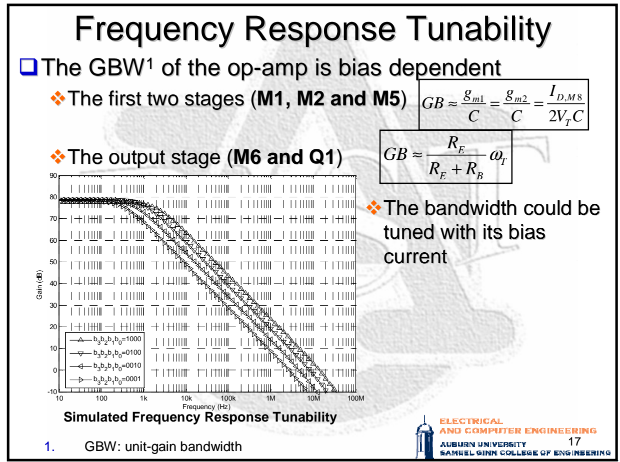
Frequency Response Tunability
The GBW[1] of the op-amp is bias dependent
The first two stages (M1, M2 and M5)
$GB \approx \frac{g_{m1}}{C} = \frac{g_{m2}}{C} = \frac{I_{D,M8}}{2V_T C}$
The output stage (M6 and Q1)
$GB \approx \frac{R_E}{R_E + R_B}\omega_T$
The bandwidth could be tuned with its bias current
Gain (dB)
Frequency (Hz)
Simulated Frequency Response Tunability
1. GBW: unit-gain bandwidth
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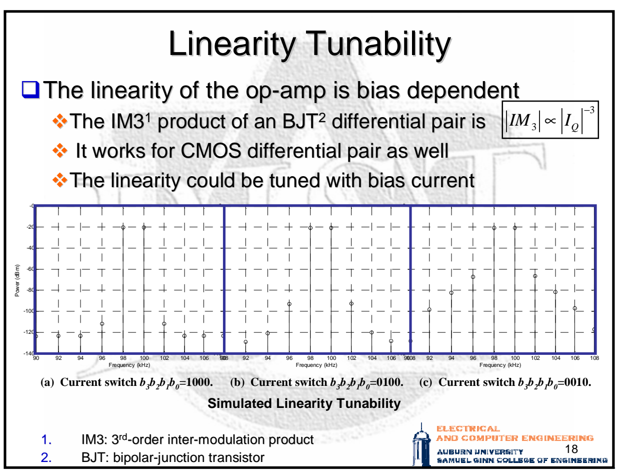
Linearity Tunability
The linearity of the op-amp is bias dependent
The IM3[1] product of an BJT[2] differential pair is $|IM_3| \propto |I_Q|^{-3}$
It works for CMOS differential pair as well
The linearity could be tuned with bias current
Power (dBm)
Frequency (kHz)
(a) Current switch $b_3b_2b_1b_0$=1000.
(b) Current switch $b_3b_2b_1b_0$=0100.
(c) Current switch $b_3b_2b_1b_0$=0010.
Simulated Linearity Tunability
1. IM3: 3rd-order inter-modulation product
2. BJT: bipolar-junction transistor
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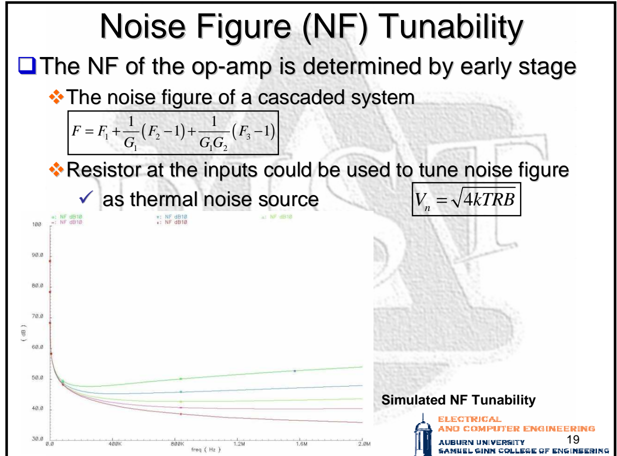
Noise Figure (NF) Tunability
The NF of the op-amp is determined by early stage
The noise figure of a cascaded system
$F = F_1 + \frac{1}{G_1}(F_2 - 1) + \frac{1}{G_1G_2}(F_3 - 1)$
Resistor at the inputs could be used to tune noise figure
as thermal noise source
$V_n = \sqrt{4kTRB}$
Simulated NF Tunability
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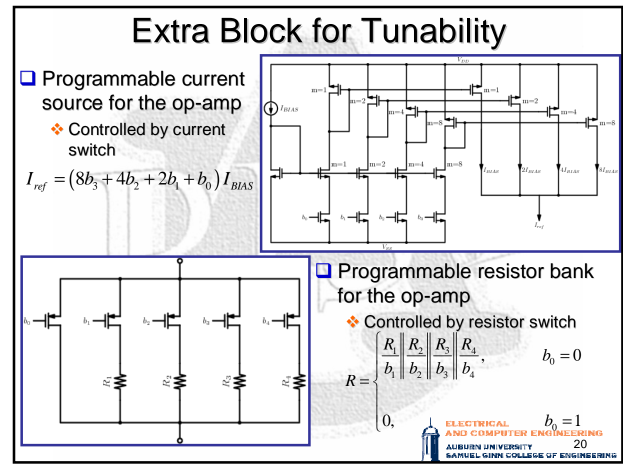
Extra Block for Tunability
Programmable current source for the op-amp
Controlled by current switch
$I_{ref} = (8b_3 + 4b_2 + 2b_1 + b_0) I_{BIAS}$
Programmable resistor bank for the op-amp
Controlled by resistor switch
$R = \begin{cases} \frac{R_1}{b_1} \| \frac{R_2}{b_2} \| \frac{R_3}{b_3} \| \frac{R_4}{b_4}, & b_0 = 0 \\ 0, & b_0 = 1 \end{cases}$
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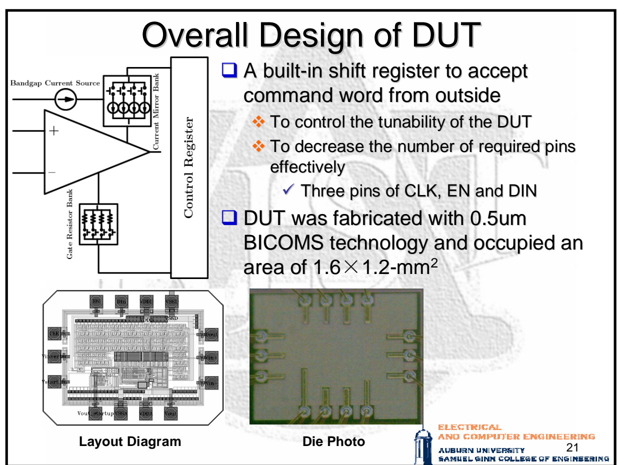

Overall Design of DUT
A built-in shift register to accept command word from outside
To control the tunability of the DUT
To decrease the number of required pins effectively
Three pins of CLK, EN and DIN
DUT was fabricated with 0.5um BICOMS technology and occupied an area of 1.6×1.2-mm2
Bandgap Current Source
Current Mirror Bank
Control Register
Gate Resistor Bank
Layout Diagram
Die Photo
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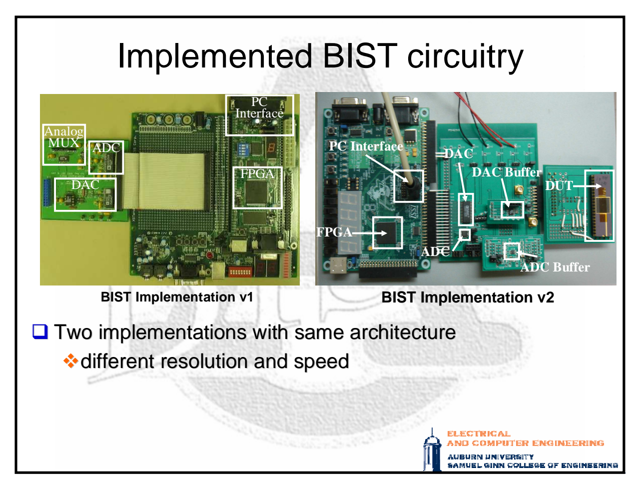

Implemented BIST circuitry
Analog MUX
ADC
DAC
PC Interface
FPGA
PC Interface
DAC
DAC Buffer
DUT
FPGA
ADC
ADC Buffer
BIST Implementation v1
BIST Implementation v2
Two implementations with same architecture
different resolution and speed
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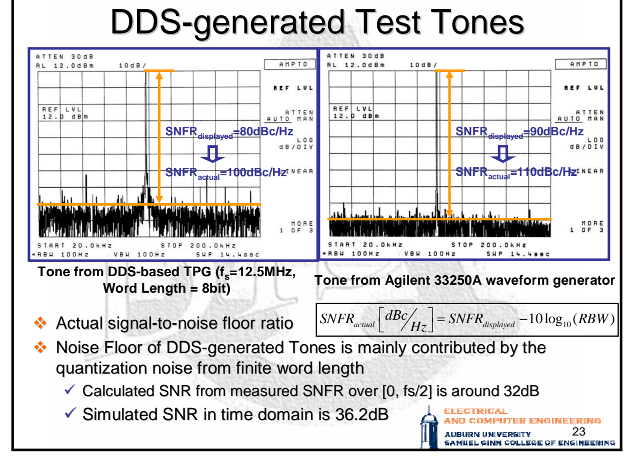

DDS-generated Test Tones
SNFRdisplayed=80dBc/Hz
SNFRactual=100dBc/Hz
SNFRdisplayed=90dBc/Hz
SNFRactual=110dBc/Hz
Tone from DDS-based TPG (fs=12.5MHz, Word Length = 8bit)
Tone from Agilent 33250A waveform generator
Actual signal-to-noise floor ratio
SNFRactual [dBc/Hz] = SNFRdisplayed − 10log10(RBW)
Noise Floor of DDS-generated Tones is mainly contributed by the quantization noise from finite word length
Calculated SNR from measured SNFR over [0, fs/2] is around 32dB
Simulated SNR in time domain is 36.2dB
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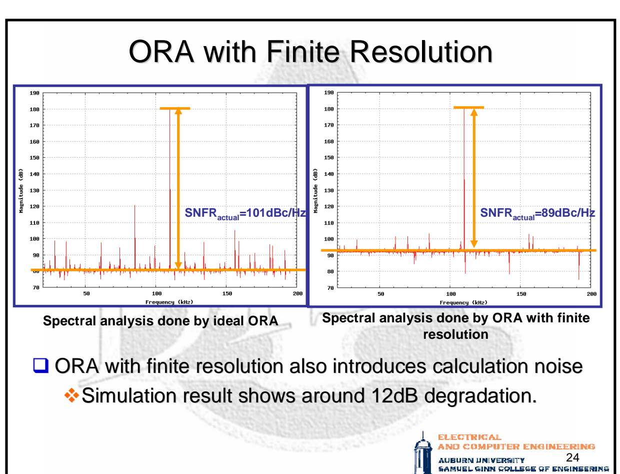

ORA with Finite Resolution
SNFRactual=101dBc/Hz
SNFRactual=89dBc/Hz
Spectral analysis done by ideal ORA
Spectral analysis done by ORA with finite resolution
ORA with finite resolution also introduces calculation noise
Simulation result shows around 12dB degradation.
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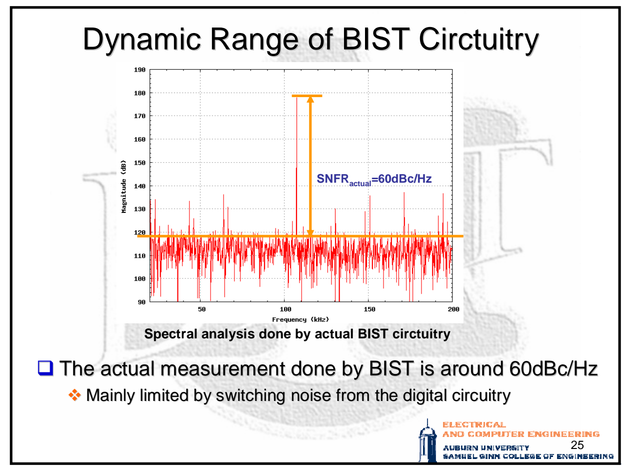

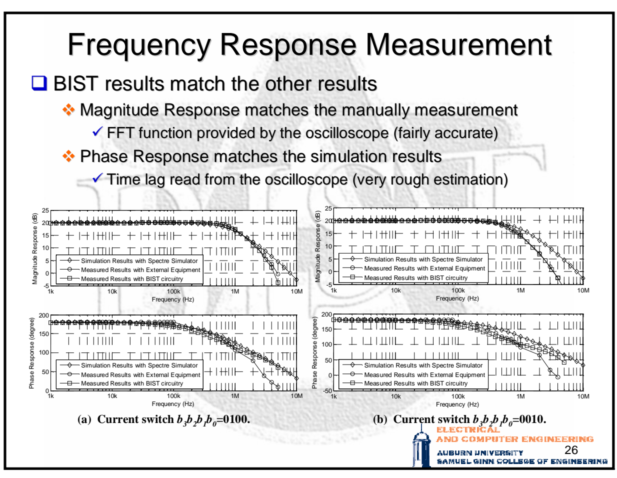

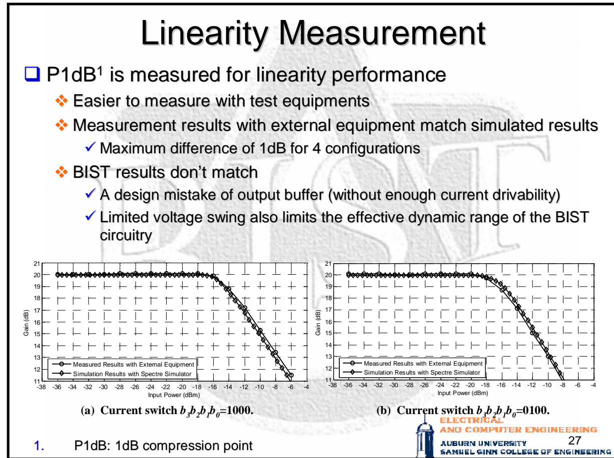

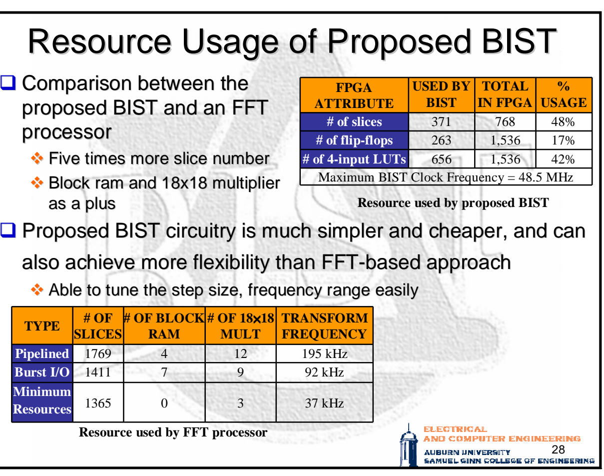

FPGA ATTRIBUTE	USED BY BIST	TOTAL IN FPGA	% USAGE
# of slices	371	768	48%
# of flip-flops	263	1,536	17%
# of 4-input LUTs	656	1,536	42%
Maximum BIST Clock Frequency = 48.5 MHz			

Resource used by proposed BIST

TYPE	# OF SLICES	# OF BLOCK RAM	# OF 18x18 MULT	TRANSFORM FREQUENCY
Pipelined	1769	4	12	195 kHz
Burst I/O	1411	7	9	92 kHz
Minimum Resources	1365	0	3	37 kHz

Resource used by FFT processor

Summary and Conclusions

- The proposed BIST circuitry is able to perform a suite of analog functional tests
  - Accurate frequency response measurement
  - Linearity and noise measurement is somewhat constrained by the effective dynamic range of the proposed BIST system
- The proposed BIST circuitry is efficient in terms of area, power consumption, and cost
- Future work
  - It is hard to apply the current architecture to RF system directly due to various practical issues
  - Goals
    - ✓ Simple analog modules
    - ✓ Work in RFIC environment

Publication List

[1]Jie Qin, Charles Stroud, Foster Dai, "Phase Delay in MAC-based Analog Functional Testing in Mixed-Signal Systems", *Proc. IEEE North Atlantic Test Workshop*, 2006

[2]Jie Qin, Charles Stroud, Foster Dai, "Phase Delay Measurement and Calibration in Built-In Analog Functional Testing", *Proc. IEEE Southeastern Symp. on System Theory*, 2007

[3]Jie Qin, Charles Stroud, Foster Dai, "Noise Figure Measurement Using Mixed-Signal BIST", *Proc. IEEE International Symp. on Circuits and Systems,* 2007

[4]Jie Qin, Charles Stroud, Foster Dai, "FPGA-Based Analog Functional Measurements for Adaptive Control in Mixed-Signal Systems", *IEEE Trans. on Industrial Electronics,* Vol. 54, No. 4, 2007

[5]Jie Qin, Charles Stroud, Foster Dai, "Test and Verification of Mixed-Signal BIST Approaches", *Submitted to International Test Conference,* 2008