**ELEC 7950-001: VLSI Design & Test Seminar**

**Broun 235, November 2, 2011, 4:30PM**

**Evaluation of a Circuit Path Delay Tuning Technique for Nanometer CMOS (Master’s Project Defense)**

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As CMOS technology approaches atomic dimensions, the unavoidable random variations in individual device parameters can critically impact high performance circuits. In a large design containing many million transistors, virtually every manufactured part will have dozens of transistors that are significant performance outliers, increasing the delay of the corresponding gate by an order of magnitude or more. Any one such device in a critical path can greatly limit the highest clock rate that can be achieved by the chip. Unfortunately, such random manufacturing variations cannot be statically addressed by better design. This project studies a design architecture that allows for the post manufacture tuning and speedup of exceptionally slow paths in a chip to recover the lost performance and significantly increase the average clock speed attainable by the manufactured parts. The key device parameter affected by random process variation is the threshold voltage (Vth). The focus of this work has been on threshold voltage variability in circuits designed with advanced CMOS logic. We present detailed simulation results for designs in 45nm NanoGate technology.

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