**VLSI Design & Test Seminar ELEC 7950-001**

**Broun 235, August 31, 2011, 4PM**

**Evaluating the Digital Fault Coverage**

**for a Mixed-Signal Built-In Self-Test**

**(MS Thesis Defense)**

**Alex Lusco**

This thesis focuses on a digital Built-in Self-Test (BIST) approach to perform specification-oriented testing of the analog portion of a mixed-signal system. The BIST utilizes a direct digital synthesizer (DDS) based test pattern generator (TPG) and a multiplier-accumulator (MAC) based output response analyzer (ORA) to stimulate and analyze the analog devices under test, respectively. This approach uses the digital-to-analog converter (DAC) and the analog-to-digital converter (ADC), which typically already exist in a mixed signal circuits, to connect the digital BIST circuitry to the analog device(s) under test (DUT). Previous work has improved and analyzed the capabilities and effectiveness of using this BIST approach to test analog circuitry; however, little work has been done to determine the fault coverage of the digital BIST circuitry itself. Traditionally additional test circuitry dedicated to testing would be added to the BIST circuitry to provide adequate fault coverage of digital circuitry. While ensuring that the digital circuitry is thoroughly tested and functioning properly, this circuitry incurs a potentially high area overhead and performance penalty. This thesis focuses on using the existing BIST circuitry to test itself by utilizing a dedicated digital loopback path. A set of test procedures is developed and analyzed which can be used to provide a set of functional tests which provide a high effective fault coverage of the digital portion of the BIST. To determine the effective of these test procedures, the mixed-signal BIST circuit is simulated and single stuck-at gate-level fault coverage results are determined and presented. Finally several improvements to the dedicated loopback path are proposed and simulated to analyze possible ways to improve the fault coverage of the BIST with minimal area and performance impact.

Contact for seminar and course:

Vishwani Agrawal, [vagrawal@eng.auburn.edu](mailto:vagrawal@eng.auburn.edu)

Seminar Series: <http://www.eng.auburn.edu/~vagrawal/COURSE/E6200_Fall11/course.html>