**VLSI Design & Test Seminar ELEC 7950-001**

**Broun 235, August 24 and September 7, 2011, 4PM**

**Built-In Self-Test for Spartan-6 Field Programmable Gate Arrays**

**(Logic & RAMs), Part I (Aug 24), Part II (Sep 7)**

**Presented by: Auburn University Built-In Self-Test (AUBIST) Laboratory**

Built-In Self-Test (BIST) for the configurable logic in Field Programmable Gate Arrays (FPGAs) was proposed in 1996. The approach exploits the re-programmability of FPGAs to configure BIST circuitry in the FPGA during off-line testing. The only overhead is the external memory required to store the BIST and system function configurations along with the time required to download and execute the BIST. No area overhead or performance penalties are incurred since the BIST logic “disappears” after the test session. Furthermore, the tests are applicable at all levels of testing since they are independent of the system function and require no external test fixture or equipment. The basic idea for the BIST is to configure some of the configurable logic blocks (CLBs) as Test Pattern Generators (TPGs) and Output Response Analyzers (ORAs) while configuring other configurable logic resources as blocks under test (BUTs). The BUTs are repeatedly configured until they have been tested in every mode of operation. These tests achieve maximal fault coverage by applying pseudo-exhaustive test patterns such that each sub-circuit of the BUT is exhaustively tested. In this seminar, we describe the development of BIST approaches for the configurable logic blocks (CLBs) and random access memories (RAMs) in Xilinx Spartan-6 Field Programmable Gate Arrays (FPGAs). A total of 14 BIST configurations are proposed to completely test the CLBs and a total of 8 BIST configurations are proposed for to completely test the embedded 18Kbit RAM modules. The CLB BIST configurations cumulatively detect 100% of stuck-at faults in every CLB while the RAM BIST configurations detect not only stuck-at faults but also pattern sensitivity and coupling faults in the RAM cores. While reuse of previously developed BIST configurations for CLBs and RAMs in Virtex-5 FPGAs is exploited, Spartan-6 FPGAs present a number of new challenges to BIST architecture, operation, and development that will be described in the presentation. Despite these challenges, novel solutions were developed, including output response analyzer (ORA) design. The implementation and experimental results of the BIST approaches in all Spartan-6 FPGAs will be discussed and demonstrated.

Contact for seminar and course:

Vishwani Agrawal, vagrawal@eng.auburn.edu

Seminar Series: <http://www.eng.auburn.edu/~vagrawal/COURSE/E6200_Fall11/course.html>