ELEC 7770-001, Spring 2014

Homework # 5

Assigned: Friday, April 14, 2014

Due: Friday, April 18, 2014

Conduct Chip Test on T2000 Tester (ATE) and Explore Power Supply Voltage versus Circuit Speed Relation

Lab instructor: Baohu Li (bzl0015@auburn.edu)

Experiment Preparation:

Tester: T2000 test system; (Locate in Broun 318)

Chip to test: 4-bit counter circuit 74LS163AN from Texas Instruments; (Placed on the test socket of T2000.)

Test patterns: Generated with ATPG tool "FastScan" to cover the stuck-at faults; (T2000 readable pattern file is placed in T2000 control PC)

OTPL (Test Programming Language) source files: Modified to support 74LS163, modifications are like vdd, vil/vih and vol/voh etc. (All source files are placed in T2000 control PC)

Automatic Test Equipment (ATE) Experiment:

1. Conduct basic stuck-at test on 74LS163AN; watch the difference in test results when test responses are identical/not identical to the expected values.
2. Using Shmoo tool integrated in the test controller see how the circuit speed is affected by the power supply voltage. (**Shmoo plot** is a graphical display of the response of a component or system varying over a range of conditions and inputs.)

Homework:

A maximum one page report is needed to be submitted by the end of this week to [bzl0015@auburn.edu](mailto:bzl0015@auburn.edu), which will be graded as Homework 5. The requirements are listed below:

1. Make a short description of the chip tested; (like technology used and electrical specifications. You can get the datasheet online and describe the relevant points.
2. Describe what you have observed in the two experimental steps.
3. You should explain what's behind your observation. Especially, discuss the Shmoo plot.

\*Details on How to Setup a Test

1. Write VHDL or Verilog code that can describe the behavior of the chip. You can use QuestaSim (or ModelSim) to verify your code through waveform or list, Invoked using the command “vsim” at the shell prompt or you can download ModelSim in you computer and verify the HDL code

<http://www.mentor.com/company/higher_ed/modelsim-student-edition>

1. Use Leonardo Spectrum to synthesis the VHDL code with a .tcl file as follows:

a. load technology library in the database

load\_library /linux\_apps/ADK3.1/technology/leonardo/tsmc035\_typ

(the library used here is tsmc035\_typ)

b. load the HDL file in the database

read {file folder/filename.vhd(or filename.v)} -format VHDL(or verilog)

c. set attribute of the ports that are defined in the HDL file

set\_attribute -port clk -name nopad -value true

d. compile/optimize design

optimize -delay(or -area)

e. generate technology specific HDL netlists

write -format VERILOG filename.v (or VHDL filename.vhd)

f. generate reports(area timing)

report\_area filename

report\_timing filename

With the .tcl file done, execute "spectrum -file filename.tcl" at the shell prompt. Then you'll get a netlist, and reports about area or timing(or both)

1. Invoke fastscan in the shell prompt "fastscan -gui" to call the GUI of fastscan, then do:
2. import the netlist file into "design"
3. import "adk.atpg" file into "ATPG Library"
4. import a dofile into "command file"
5. then click "invoke fastscan", and run the fastscan, you can get a .pat file that contains vectors. <http://www.eng.auburn.edu/~nelson/courses/elec5250_6250/>
6. For the use in T2000 machine, you need to change the format of the vectors into the format that T2000 can identify; refer to the file "estimation of maximum frequency of operation" in VLSI testing Lab.
7. Have all the otpl source files in your own folder, maintaining the directory structure and names. (Refer to Dr. Nelson's slides "T2000 Seminar Spring 2014" on website)
8. Generate the env file for the t2kctrl: run "make\_settings\_env.bat" in your working folder, the env file named "settings.env" will be generated.
9. Set environment variables for pattern compiler: replace "%1" in "SetEnv.bat" with your working directory address, then run it.

8. Compile pattern file: in cmd prompt, go into the "Patterns" directory in your working directory, enter:

"oai\_patcom -s socket.soc pat1.pat", Compiling the pat file. An .pobj file with the same name with .pat will be generated.

1. Go back to your working directory, enter: "t2kctrl start" to invoke T2000 controller.
2. Load test plan: selecting the .tpl file in the "otplsrc" directory; the socket.soc in the "testplans" directory; Settings.env in the working directory. Load.
3. To run the test and monitor test result, refer to "estimation of maximum frequency of operation".