ELEC 7770-001, Spring 2012

Class Project

 Assigned 4/2/2012

Class Presentations 4/23/2012 and 4/25/2012

Final Report due 4/27/2012

Work to be performed either individually or in a group of no more than two students.

Problem: Design the fastest possible 32-bit 2’s complement integer adder in 180nm CMOS technology.

Class Presentation, five minutes each, 4/23/2012 or 4/25/2012; use only three slides:

1. Algorithm and architecture.
2. Tabulated performance data.
3. Conclusion.

Email slides to vagrawal@eng.auburn.edu after the presentation.

Report, submitted as an electronic file no later than 4/27/2012, should contain the following:

1. Algorithm implemented, with reasons for the choice.
2. List any tools used.
3. Describe how functional correctness of the circuit was verified. Do not include any printouts.
4. Describe how the delay of the adder was determined.
5. Tabulate design data: numbers of gates, inputs and outputs; critical path delay; minimum delay;
6. Conclusion: Briefly discuss what was accomplished, what you learnt, and what can be improved.
7. References
8. Appendix: Include HDL description.