[[1]](#footnote-1)

**STUDY OF PROCESS VARIABILITY ON PERFORMANCE AND POWER**

Mridula Allani Spring, 2010

*Abstract*— With the reduction of MOSFET dimensions, the manufacturing process variations have been increasing in the CMOS technology. For example, the intra-die variations in channel length were observed to be 35% of total variations in 130nm CMOS and 60% in 70nm CMOS [5]. The variations in the impurity doping concentrations, oxide thickness, temperature, channel length and other process parameters affect the electrical parameters such as delay, node capacitances, threshold and currents in the transistors. In this project, I have studied the effect of threshold voltage variations on the delay, dynamic power and leakage power in a two-bit ripple carry adder. Monte Carlo Analysis has been used to simulate the variations in 45nm and 32nm CMOS technology.

*Index Terms*— Dynamic Power, Leakage Power, Critical Path Delay, Monte Carlo Analysis, Process Variations, Threshold Voltage, 3-sigma Deviation.

# INTRODUCTION

Power and performance are the most important design considerations for the digital designers. Various design techniques have been developed to optimize power and performance for electronic circuits. The threshold voltage, oxide thickness, and the channel length are the most important parameters that effect the power consumed by a device and its speed of operation. These parameters are now subject to stochastic variations induced by the semiconductor process and hence, is largely impacting the device operation.

The semi-conductor manufacturing process induces some variations in the physical parameters of the MOS devices which in turn induce variations in the electrical parameters of the devices. These variations are statistical in nature. Due to shrinking of technology node these process variations are introducing very drastic variations in the electrical properties of the MOSFETs and thereby affecting its performance and power distribution.

The parameters that get affected are, but not limited to, the doping concentrations, the oxide thickness, the gate length and width, the threshold voltage, the channel length, propagation delay and power dissipation.

According to authors of [3], the variation in threshold voltage for a 45nm CMOS process is about 42% and the variations in channel length is about 10%. Authors of [5] quote that the intra-die variations in channel length were observed to be 35% of total variations in 130nm CMOS and 60% in 70nm CMOS. It is observed that there is an increasing trend in the variations with decreasing technology node. The trends in various parameter variations are discussed in [2]and shown in Figure 1.

The process variations can be intra-die or inter-die. The inter-die process variations are the variations across the wafers or wafer-lots. And the intra-die variations are the variations within the die. These variations effect the yield of a CMOS process and it is important to properly estimate the amount of variations for each process and proper measures have to be taken to minimize these.

Various environmental factors contribute to these process variations. They include the power supply fluctuations, the operating temperature, the delay-induced cross-talk and other on-chip noise sources. The physical and electrical parameters of the MOSFETs are subjected to variations due to the variations caused by the fabrication process and the device wear-out mechanisms.

The inter-die variations are modeled using worst-case corners or Monte Carlo Analysis. The intra-die variations are not yet modeled accurately and involve intricate dependencies between the process parameters. The inter-die variations do not depend on the design-implementation, but the intra-die variations depend on the die layout and hence the logic design.

**TABLE 1. Typical values of technology parameters.**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|   | **Vdd(V)** | **Vth0n (V)** | **Vth0p (V)** | **Delay(s)** | **Leakage Power (W)** | **Dynamic Power(W)** |
| **45nm** | 1 | 4.69E-01 | -0.49158 | 5.51E-11 | 2.00E-07 | -2.00E-07 |
| **32nm** | 0.9 | 4.94E-01 | -0.49155 | 4.02E-11 | 2.43E-07 | -2.43E-07 |

**TABLE 2. Percentage 3-sigma variations in 45nm tehnology parameters.**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **3-sigma variation in Vth (mV)** | **Vth0n (V)** | **Vth0p (V)** | **Delay (s)** | **Leakage Power(W)** | **Dynamic Power(W)** |
| 10 | 2.219445 | -2.02529 | 2.331818 | 16.41062053 | 0.407829296 |
| 30 | 6.648999 | -6.07933 | 6.720632 | 51.37083603 | 1.89192687 |
| 50 | 11.08148 | -10.1245 | 10.5746 | 92.26371429 | 2.915445036 |
| 100 | 22.16777 | -20.2481 | 20.19053 | 248.824085 | 6.092179777 |
| 200 | 44.33608 | -40.5001 | 43.02196 | 1176.046942 | 14.21211229 |

# Project Description

In this project a two-bit ripple carry adder is designed. An RTL level net-list is generated from the Verilog HDL code using Leonardo Spectrum and then a transistor level net-list is obtained by using Design Architect. The schematic is shown in Figure 2. The power dissipation and critical path delay are measured form HSPICE simulations. The Predictive Technology Model cards for 45nm and 32nm technologies are used for the simulations.

The input vectors used to activate the critical path of 

**Fig. 1. Trends in parameter variations. [2]** **Sani R. Nassif, IBM Austin Research Laboratory.**

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**Fig. 1. The figure shows a two-bit ripple carry adder each of whose sub-circutis are full-adders..**

the ripple carry adder are {11, 00, 0} and {11, 00, 1}.

The delay is measured as the time difference between the 50% transition point of the output carry and the 50% transition point of the input carry. The leakage power is measured for the vector set {11, 00, 1}. And the dynamic power is measured as the difference between the total average power and the leakage power.

The threshold voltage variations are modelled as Gaussian distribution. The 3-sigma variation in the threshold voltage is varied as 10mV, 30mV, 50mV, 100mV and 200mV for both 45nm and 32nm technologies. Each model is subjected to a 100 Monte Carlo runs in HSPICE and the results are tabulated. The 3-sigma variations of the delay and powers are calculated for each model. Then the percentage

**TABLE 3. Percentage 3-sigma variations in 32nm tehnology parameters.**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **3-sigma variation in Vth (mV)** | **Vth0n(V)** | **Vth0p(V)** | **Delay(s)** | **Leakage Power (W)** | **Dynamic Power (W)** |
| 10 | 2.101845 | -2.02393 | 2.441912 | 16.50946 | 1.260096 |
| 30 | 6.310868 | -6.07425 | 6.992713 | 51.29022 | 3.790551 |
| 50 | 10.52554 | -10.1243 | 11.42354 | 91.51881 | 6.527123 |
| 100 | 21.04386 | -20.2575 | 23.15968 | 245.6372 | 13.68903 |
| 200 | 42.09039 | -40.5092 | 50.4828 | 1232.871 | 32.3105 |

variations of these parameters is calculated by comparing with the typical values of the respective parameters obtained from simulating the models with constant typical threshold voltage.

# Experimental Results

The typical values of the technology parameters for 45nm and 32nm process are listed in Table 1. The percentage 3-sigma variations in the technology parameters are listed in Table 2 for 45nm process and Table 3 for 32nm process.

The variations can also be seen in Figure3 for 45nm and Figure 4 for 32nm technology at the end of the text. The first series in these figures is the the critical path delay, the second series is the leakage power and the third series is the dynamic power. We observe that the variations in leakage power are very large compared to the variations in dynamic power and the critical path delay. Also, we note that the variations in all the three parameters increase as the technology is decreasing.

The variations can also be seen in the Monte Carlo scatter graphs for each of the parameters in Figures 5-6 at the end of the text.

# CONCLUSIONS

 We observe that the variations in leakage power increase exponentially when compared to the variations in delay or dynamic power with the increasing variations in threshold voltage. Hence, it is very important to determine the permissible variations in process parameters in the nano-scale CMOS process. And it is equally important to develop new ways of limiting these variations.

# FUTURE WORK

 The variations in critical path delay and power have been studied with the variations in threshold voltage for 45nm and 32nm two-bit ripple carry adder circuit. It would be interesting to see these trends for larger circuits. Also, the effect of variations in other process parameters can be similarly studied. The correlation between the variations in nMOS and pMOS parameters have to be considered and an accurate statistical model for the transistors can be used for simulations.

References

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**Fig. 3. Percentage 3-sigma variations in 45nm tehnology parameters. The first series in these figures is the the critical path delay, the second series is the leakage power and the third series is the dynamic power.**

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**Fig. 4. Percentage 3-sigma variations in 32nm tehnology parameters.** **The first series in these figures is the the critical path delay, the second series is the leakage power and the third series is the dynamic power.**



**Fig. 5. The scatter plots for the 45nm parameters.**





**Fig. 6. The scatter plots for the 32nm parameters.**

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