**ELEC 7770** **Advanced VLSI Design HW-4**

Submitted by Mridula Allani

“Architectures for Silicon Nanoelectronics and Beyond,Computer, vol. 40, no. 1, pp. 25-33, January 2007.”

* R. I. Bahar, D. Hammerstrom, J. Harlow, W. H. Joyner Jr., C. Lau, D. Marculescu, A. Orailoglu and M. Pedram

The authors discuss the issues that might affect the design, architecture, and reliability of electronic circuits in the technology succeeding the CMOS. With the CMOS scaling approaching the physical limits, many new molecular-scale devices are being considered to improve device density, performance, power-density, energy-efficiency and complexity of electronic circuits. These new technologies include carbon nanotube transistors, carbon nanotube devices, molecular electronics, spintronics, quantum-computing, magnetic memory devices, optoelectronics, etc. Some hybrid systems which are also called modified-CMOS devices are also being considered which integrate the conventional CMOS with the previously mentioned new technologies. These devices might have different logic primitives and fault models than the conventional CMOS logic.

While enhancing a few important design parameters, these nanoelectronic devices introduce new problems. The new nano-scale devices will not be used until there is absolutely no scope for CMOS to bring profits. These devices also need to demonstrate sufficient reliability and large-enough signal-to-noise ratio to guarantee reliable digital computation. New semiconductor process, device models, and analysis, simulation, verification and optimization techniques and tools are required to fabricate inexpensive and reliable chips. The noise generated, exact behavior at different operating conditions, fault modeling, analysis, and statistical nature of these devices are still unknown. New architectures and design processes must be explored to make effective use of such devices.

Large process variability in these devices produces low yields. These devices also have high soft-error rates due to reduced noise-margins and produce operation uncertainties due the probabilistic switching. Because of the unreliability of these devices, defect rates and process variability will become first-order design considerations in such devices. In some of these devices, switching is accomplished without the need to move charge in space. Such architectures will be more complicated and will require redundancy at several levels of abstraction for fault tolerance.

References:

1. A DeHon, KK Likharev,*”* *Hybrid CMOS/nanoelectronic digital circuits: devices, architectures, and design automation,“* Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design.

2. R. K. Cavin, V. V. Zhirnov Contact Information, G. I. Bourianoff, J. A. Hutchby, D. J. C. Herr, H. H. Hosack, W. H. Joyner and T. A. Wooldridge,” A Long-term View of Research Targets in Nanoelectronics,” Journal of Nanoparticle Research (2005) 7: 573–586.