04/05/2010 Priyadharshini S.

Advanced VLSI Design – Homework 4

**The High-k Solution**

Authors: Mark T. Bohr, Robert S. Chau, Tahir Ghani, Kaizad Mistry

a) Important points the authors make:

1. With new generations, the insulation material used in transistors had become too thin and could not be made any thinner. This was also leading to unnecessary power dissipation due to leakage caused by electron tunneling through the insulation layer. A material with high k (dielectric constant) could solve the problem since it would provide the same capacitance with higher thickness [1].

2. Hafnium- and zirconium- based dielectrics, deposited by the atomic layer deposition technique [2], exhibited the required stable electrical characteristics.

3. Metals were found to be the appropriate gate material [3] that would work well with the new insulating layer. The work function of these metals had to be modified so that the threshold voltage of the transistors was appropriate.

4. The NMOS and PMOS transistors required different gate materials due to the differences in their electrical properties.

5. Metals cannot withstand the high temperatures used in the annealing step [4], if the gate-first fabrication method were to be employed. Therefore, the gate-last technique was employed.

6. Penryn processors fabricated recently have transistors’ features measuring around 45 nm, though one is as small as 35 nm.

b) Impact on the future:

1. Transistors with lower leakage can be manufactured at 45-nm. Thus, they would expend lesser power.

2. The transistors would be faster because of the use of metal gates.

3. The transistors work much better than their predecessors, and can be scaled further to 32-nm.

c) Main roadblocks in widespread use:

1. Researchers see the gate-last process adopted, as too much of a departure and too challenging.

2. New materials and structures might be needed to scale these transistor structures to the next two generations – 22-nm and 16-nm.

References:

1. Wikipedia article titled High-k dielectric.

2. Ritala M, Leskela M. 2002. Atomic layer deposition. In *Handbook of Thin Film Materials*, ed. HS Nalwa, Vol. 1, pp. 103–59. San Diego: Academic

3. Chau, R. et al. High-k/metal-gate stack and its MOSFET characteristics. *IEEE Electron Device Letters* 25, 408–-410 (2004).

4. Article in webpage http://www.intel4004.com/sgate.htm