Prardiva Mangilipally

Computing with Trillion components:

* This paper starts with the discussion of the possibility of building machines that could operate perfectly even when the components are defective or unreliable.Earlier computers were built using vacuum tubes and relays which were highly unreliable due to which computations had to be rerun multiple times whenever there was a component failure.So the scientists seriously examined the possibility of defect tolerant machines until the advent of integrated circuits which were highly reliable.The need for exploring the possibility of building defect tolerant circuits has begun to increase again in the recent past due to the drastic shrinkage in device sizes.This is the main **motivation** of the paper.
* As the size scales less than 22nm the operation of transistors has become problematic.So a need for new types of switching devices will be explored in the future circuits either individually or in combination with transistors.One such solution has been proposed by the author.These switches have very different operating characteristics from standard silicon devices and are built from small clusters of molecules(very few) or a very thin layer of an oxide material between two metal electrodes.They are nanometer-sized electrochemical cells that can be toggled open (high resistance)or closed (low resistance) by placing a potential across the device that exceeds a threshold voltages.The opening and closing threshold voltages usually change the electrical resistance.These Switches can be utilized as the basis for a memory or a logic circuit but the challenge is wiring up a huge number of them(order of trillions) to perform a useful task and manufacturing very small wires.So to overcome the above problem a process called nano imprint lithography has been suggested to build nanometer-scale circuits .using this we can make nanowires that are approximately 15nm wide.A self-assembling and self-aligning techniques are used to assemble the switches and connect them.
* Hybrid technology combines both nanoscale switches & microscale CMOS and is called Field-programmable Nanowire interconnect. The basic idea is to make a hybrid nanoswitch/CMOS chip, using the switch components only for configurable interconnect, and using standard CMOS microcircuitry for all other functions, such as logic and configuration of the interconnect .Compared to the standard FPGA architecture, this approach takes all of the CMOS resources required for the configuration bits and switches and replaces them with a set of nonvolatile nanoswitches residing in the metal interconnect layer. Since nanoswitches are much smaller than the configuration bits that consume a large fraction of the area in a traditional FPGA, this design offers much greater logic density.In a recent study , FPNI circuit has been described to have an eight factor increase in logic density,comparable clock speed and reduced power dissipation compared to a CMOS only FPGA, using the same transistor technology.**This improvement is equivalent to three generations of CMOS development, or nearly 10 years equivalent to Moore’s Law technological progress, without having to shrink or improve the transistors in the circuit.**
* Hybrid technology is quite promising and helps us overcome the limitations of CMOS technology such as optimizing the metal interconnect, which is a major performance limitation in terms of operating speed and power dissipation.The dense interconnectivity,high bandwidth,uniformity, and sparse utilization of the nanowire crossbar enables very effective schemes for defect tolerance. Hence it is advantageous to introduce hybrid technologies,in which some type of nanoscale switch is used to complement CMOS, and thereby continue Moore’s Law rates of improvement in computing capacity while maintaining reliability for many more decades into the future with only modest improvements in transistors.

**REFERENCES:** **Dmitri B. Strukov, Konstantin K. likharev. *A reconfigurable architecture for hybrid CMOS/Nanodevice circuits***.

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