Summary

Homework1 ELEC7770

Student Name: Binying Tan

Today computer hardware technology is based on silicon and the technological trend in the semiconductor industry continue to abide by Moore's Law, but the continually shrinking size of circuitry packed onto silicon chips would eventually reach a point where individual elements would be no larger than a few atoms and eventually the conventional wisdom of transistor cramming for progress must be abandoned. So as we are getting close to the end of this roadmap, we have to prepare ourselves further for our computing-power-demanding future.

Part One

The first article [1] addresses some new computing paradigms that we have already begun to explore.The research for these new paradigms are basically multi-discipline, especially both physics and chemistry are enormously involved in the implement . But as time goes by, we believe that more and more efforts will be made on architectural design, schemes and algorithms.

1 Atomic,molecular and quantum computing

Distinguishing themselves from traditional computer hardware,these computers will be built in a "bottom-up" way,starting at assembling their basic elements. We could possibly achieve a local device density of one trillion elements per square centimeter.

Speed: Potential speeds can be in the pico-second range such as computing by carbon nanotubes.

2 Molecular, chemical and organic computing

For example, DNA computing is performing bio-molecular processes to achieve computing while the information is encoded on DNA.

Speed: Although the single element speed is rather slow (in the order of 100~1000s), compared with its carbon nano-tube brethren, the overall speed will be significantly faster because its highly parallel scheme.

3 Optical computing

So far logic gates such as AND and XOR have been built but cascading issue ramains unresolved.

Speed: The speed could leap to the order of femto-sencond and if it is used in conjuction with traditional silicon-based technology, it can enhance the overall speed.

4 Other special forms:Micro/nanofluidics computing; Neurocomputing;

Part Two

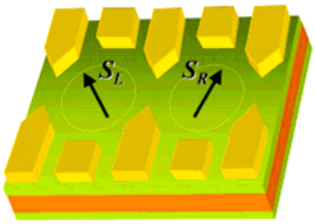
Each paradigm's fundamental nature requires specific algorithms and thus will change the forms of information processing and applications.Regarding quantum computing, extra readings lead to the following undersandings.

1 The history of exploration of quantum computing

The idea of a computational device based on quantum mechanics was first explored in the 1970's and early 1980's by physicists and computer scientists when scientists were pondering the fundamental limits of computation. Richard Feynman came up with the concept of quantum computing because the simulation of the dynamics of quantum systems on conventional computers is hard, meaning that the computational resources needed to simulate a quantum system increase exponentially with its size. One of the first practical quantum algorithms was presented by David Deutsch and Richard Jozsa in 1992. Then 1994 quantum computation captured world-wide attention, as Peter Shor presented his quantum algorithm for the prime factorization of integers. By this algorithm we can get an exponential speedup which is a fundamental breakthrough in computational complexity.Other recent quantum algorithms include those estimating Gausssums, solving certain hidden shift problems, efficient gradient calculation, and counting points on certain curves.

2 Basic concepts

As its counterpart in classical computation, a qubit is the basic unit of information in quantum computation. The qubits in the figure are formed from the two spin states ($|\uparrow, |\downarrow$) of a confined electron. In contrast with traditional concept of state 1 or state 0, a quantum system could be in both by entanglement. Besides, a quantum computation is performed through a set of transformations, called gates. A gate applies a unitary transformation U to a set of qubits in a quantum state. It can be shown that it is possible to construct such a set with gates that act only on one or two qubits at a time. A typical universal set is a single gate transform plus a CNOT or SWAP.



DiVincenzo (IBM) proposed 5 criteria should be fulfilled to implement a quantum computer:Information storage: (1) stable memory; (2)Preparation for initial state (0000); (3)Isolation: The quantum nature of the qubits should be tenable; this will require enough isolation of the qubit from the environment to reduce the effects of de-coherence; (4)Gate implementation: We need to be able to manipulate the states of individual qubits with reasonable precision, as well as to induce interactions between them in a controlled way, so that the implementation of gates is possible. Also, enough isolation of the qubit from the environment is required to reduce the effects of decoherence. That is the gate operation time τ_s has to be much shorter than the decoherence time T_2, so that $\tau_s/T_2 \ll r$, where r is the maximum tolerable error rate;(5) Readout: It must be possible to measure the final state of our qubits once the computation is finished, to obtain the output of the computation.

3 Experimental implementations.

There appears no theoretical obstacles to building a large-scale quantum computer after developing quantum error correction and fault-tolerant quantum computation.In the past years, different methods are exploited such as superconducting circuits, NMR, ion trap,trapped neutral atom, photons and coupled quantum dots. So far ion-trap quantum computers are with up to eight qubits and NMR quantum computers with up to 12 qubits. The proposals based on solid-state qubits have demostrated the basic one- and two-qubit manipulations necessary for quantum too. Since the scalability is very important concern, Solid-state qubits are very promising because they could take advantage of existing technology.

4 Quantum cryptography.

MagiQ and idQuantique, are marketing the first generalization quantum key distribution devices.

Part Three

Although we are mainly focusing on implementation today as stated above, it is suggested that research into the architectures, methods and tools should be carried out at the same time . Article 2 addresses how new computing paradigms could change the way we design a system, especially a hybrid one, since all the novel devices won't be a replacement technology of silicon-based circuits right way.

1 The definition of nanoarchitecture.

The organization of basic computational structures composed of nanoscale devices assembled into a system that computes something useful.

2 The revolutionary path

We've been on an evolutionary path for a long time, improving the performance by increasing the element density on a chip as well as solving the issues such as power consumption and heat dissipation. Soon or later we'll switch to a revolutionary path.

New devices, in the forms of carbon nanotube transistors, carbon nanotube memory devices, molecular electronics, spintronics,quantumcomputing devices, magnetic memory devices, and optoelectronics, have intrinsic properties, which are different from their traditional counterparts. We expect them to operate at reduced noise margins, thereby exposing computation to higher soft-error rates.So the new systems require that: Reliability; Tight synergy between levels of technology abstraction and well-designed interface between them;

Architecture

The goal is to design reliable, cheaper, and better performing architectures built from hybrid nano-electronic circuitry, it's not clear what aspects of current architectures will present the most serious constraints. So far, globally asynchronous, locally synchronous (GALS) design seems to be a favorable approach. Further, to address the

fault tolerance and redundancy issue, we need to pay attention to new devices' noise behavior. Low power is one of strong points of nanostructures but at the same time this expose the system in the sea of thermal fluctuation. And the variation between devices due to pre-matured fabrication could be larger. So although temporal and hardware redundancy have traditionally resolved high fault rates, allowing a small number of faults to be visible at the software level could be a much cheaper solution. The Granularity of the fault tolerance is also important. Both reliability theory and computational theory on coding technique and re-configuration need to be further developed in order to do the fault/defect management.

3 The driven Force

Application is the driven force, which shapes the computer architecture of a hardware system to provide a reasonably efficient solution to a variety of application problems. 3 most often seen domains are mostly in the multimedia, communication, and pattern-recognition. For example, to mimic biologically auditory processing, in addition to dense memories and massively parallel processing, nanoelectronics could offer the potential for combining the sensing of sound and the processing of speech into a single computational nanoarchitecture. In another word, hybrid architectures might allow for integration of sensing with logic and memory.

4 Challenges

Models of new devices have yet to be developed to aid the circuit design;
Logic primitives;
Circuit fabrics;
Defects.
Terascale integration;
Design flow and design tool;

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