01-17-2008 Mohammed Ashfaq Shukoor

Advanced VLSI Design
Homework 1

Summary of the articles:

1. ***Beyond Silicon: New Computing Paradigms***
2. ***Architectures for Silicon Nanoelectronics and Beyond***
3. ***Autonomous Programmable Biomolecular Devices using Self-Assembled DNA Nanostructures***

Today, the microelectronic industry faces serious challenges in keeping up to the Moore's Law, according to which the computing speed and memory capacity doubles every 18 months. All past improvements in computing speed and memory size have been achieved by reducing the transistor size. Presently the sizes have become so small that semiconductor devices are haunted by power density, interconnect scaling, defects and variability issues. It is anticipated that further advancements will slow down and come to a halt during the next 5 to 20 years period.

Sensing the urgency of need for post-CMOS technologies for information processing to sustain Moore's Law, many scientists have embarked on research to find alternatives to silicon based technology.

The research and development work for these new paradigms is in preliminary stages and has mostly been reported in literature outside of the computer science and electrical engineering disciplines, such as physics and chemistry. However, as these technologies become more advanced, there are more opportunities for computer scientists to become involved. One area is the hardware aspect of the technologies, such as architectural design. Another is the software aspect, developing computing schemes and algorithms specific to these technologies.

The article [1] briefly discusses the two categories of computing schemes. The first one is based on nanoscale technology; the areas covered include computing schemes based on carbon nanotubes, organic molecules, bio-DNA, and quantum physics. The second is about special forms of computing that includes optical and micro/nanofluidic techniques.

1. Atomic, Molecular, and Quantum Computing:

In this case the basic computing elements are atoms and molecules of nanoscale. Computers will be built by assembling these elements following a bottom-up approach. This is in contrast to the top-down approach followed for the current silicon based technology.

Carbon Nanotubes:

Carbon nanotubes with attractive features such as nanometer sized diameters, speeds in the pico-seconds range and less electron scattering are potential devices for the next generation computing components. Basic logic gates such as NAND and NOR, and memory cells have been constructed. Integrating these gates to create more complex devices is yet to be implemented, and this would be a major breakthrough for this technique to become a full-scale computing technology.

***DNA Computing*: (*Summary of article [3]*)**

The molecular-scale devices covered under this topic are DNA nanostructures. The following points give a gist of the DNA structure

- DNA is made up of subunits called nucleotides.
- Each nucleotide is made up of a sugar, a phosphate and a base.
- The DNA backbone is formed by the sugar and phosphate units.
- There are 4 different bases in a DNA molecule:
  adenine (A), cytosine (C), guanine (G), thymine (T)
- The bases are grouped into complementary pairs (G, C) and (A, T).

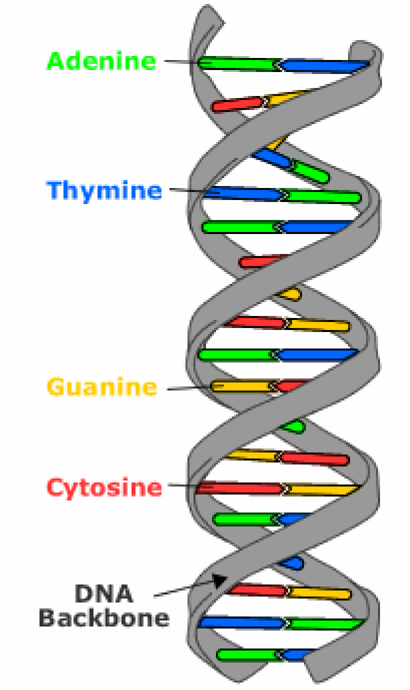

Figure 1: DNA Double Helix

The most basic DNA operation is hybridization, where two single-stranded DNA (ssDNA) oriented in opposite directions can bind to form a double-stranded DNA helix (dsDNA) by pairing between complementary bases. DNA hybridization occurs in a buffer solution with appropriate temperature, pH, and salinity. The kinetics of the DNA hybridization process is quite well understood and can be approximated by known software packages

A DNA nanostructure is a multi-molecular complex consisting of a number of ssDNA that have partially hybridized along their sub-segments. They are constructed primarily of synthetic DNA. A key principle in the study of DNA nanostructures is the use of self-assembly processes to actuate the molecular assembly. Here autonomous self assembly is important because the DNA nanostructures can be produced without any tedious laboratory setups and little external mediation.

The reasons for using DNA to assemble molecular-scale devices are

- The geometric and thermodynamic properties of ssDNA are well understood and can be predicted by softwares by analyzing parameters such as sequence composition, temperature and buffer conditions.
- A DNA nanostructure or device can be designed from a library of ssDNA strands with specific segments that hybridize to (and only to) specific complementary segments on other ssDNA. There are a number of software systems (developed at NYU, Caltech, and Duke University) for design of the DNA sequences composing DNA tiles and for optimizing their stability.
- The assembly of DNA nanostructures from ssDNA is a very simple experimental process
- In addition to the hybridization reaction, there is a wide variety of known enzymes and other proteins used for manipulation of DNA nanostructures in a predictable manner.
- The assembled DNA structures can be characterized by techniques such as electrophoresis, Atomic Force Microscopy (AFM), Transmission Electron Microscopy (TEM)

The first experiment on DNA computation was performed by Addleman in 1994. He used DNA nanostructures to find a Hamiltonian path in a graph, which is a path that visits each node exactly once.

Another idea of DNA computation by self assembly was proposed by Winfree according to which, tiles composed of DNA could be used to perform computations during their self assembly process. A DNA tile is a DNA nanostructure that has a number of sticky ends *(is an unhybridized ssDNA protruding from the end of a double helix on its sides),* which are termed as pads. The DNA tiles are assembled together my hybridization of their pads. The pads of the tiles are designed such that the tiles assemble as intended. The first experimental demonstrations of computation using DNA tile assembly was [5]. It demonstrated a two-layer, linear assembly of DNA tiles that executed a bit-wise cumulative XOR computation.

The computing speed of a single basic element in DNA computing is slow, in the order of 10^2 to 10^3 seconds, but parallel usage of a very large number of such elements could significantly improve the overall effective computing speed.

Molecular-scale devices using DNA nanostructures have also been engineered to have various capabilities, including: execution of molecular-scale computation; use as scaffolds or templates for the further assembly of other materials such as scaffolds for various hybrid molecular electronic architectures or perhaps high-efficiency solar cells; robotic movement and molecular transport; exquisitely sensitive molecular detection; amplification of single molecular events; and transduction of molecular sensing to provide drug delivery.

Quantum Computing:

It is based on quantum physics. Here a quantum bit or qubit is the basic unit of information which can be a 0, 1 or a superposition of 0 and 1 at the same time. Quantum computing has been applied to a variety of computationally difficult problems, including search, cryptography, and number theory.

2. Special Computing Schemes:

Optical Computing:

It could revolutionize the computing speed to the order of femto-second (10^{-15}) which is 10^5 times faster than current silicon based technology. While a specific computer architecture has yet to be constructed, logic gates such as AND and XOR have been built, and an all-optical half adder was reported recently as well.

***Micro/Nanofluidics**:*

Micro/nanofluidic computing is a special-purpose computing model incorporated on small-scale fluidic platforms. Its advantages are, processing times are typically much shorter than equivalent macroscale processes; thousands of channels can be placed on a small planar surface (lab-on-a-chip) allowing for parallel operations; and the sizes are close to those of individual cells and molecules. Its potential applications include areas such as biomedicine and engineering.

The article [2] discusses about need and ways to develop nanoarchitectures so that systems based on nanoelectronics can be created effectively.

Nanoelectronics has a potential to put a trillion molecular-scale devices in a square centimeter. But, making a single device to work and making millions of them put together to work are two very different things. In addition to how to assemble these tiny devices, one major challenge is to produce reliable systems from unreliable components with unpredictable behavior. Thus effective use of nanotechnology will require not just solutions to increased density, but total system solutions. Thus we need to develop circuit fabrics that can coordinate this enormous number of devices so as to perform useful computations.

In addition to Nanoelectronics based systems, scientists are pursuing integration of nanoelectronic devices with CMOS based digital logic to create hybrid systems.

Nanoarchitecture is defined as the organization of basic computational structures of nanoscale devices into a system that can perform some useful computation. There are some issues that need to be addressed while designing the nanoarchitectures for reliable computing systems from unreliable devices. These are as follows,

Defect and Fault rates: One of the major problems with future nanoelectronic devices is high manufacturing defect rates due to inherent stochastic switching behavior of the devices. Since it is impossible to replace or repair any of these nanoscale components, the need for reliability will be met through redundancy of the nanowires and switches. Applied cleverly, a relatively small amount of redundancy can provide a substantial amount fault tolerance in the circuits. Also error detection and correction should be incorporated at various levels of abstraction to achieve fault tolerance.

Fault Models: Detecting faults requires incorporation of an effective test-design methodology into the architecture. Thus new fault models need to be developed that do realistic characterization of the nature of faults at the molecular scale.

Probabilistic Computation: Nanoscale devices are intrinsically error prone because thermal fluctuations can easily switch their logic states. Thus the computation with such devices becomes probabilistic in nature. Researchers have to develop architectures by taking the probabilistic implementation into account.

Reliabiltiy: Unitil now circuits have been optimized based on the area, delay and power aspects. But for the nanoscale devices, reliability of the system must also be considered.

Applications: The applications that the nanoscale devices will execute should be an important consideration for the design of nanodevice architectures and circuits,

Hybrid nanoelectronics in which nonvolatile, fast nanoelectronic memory devices are integrated with very dense conventional silicon technology make fascinating hybrid architectures possible. The availability of extensive local storage, fully integrated with logic, could offer new capabilities and increased performance for applications currently limited by the logic-memory communication. One class of applications would be vision systems in which each photo detector is embedded with its own circuitry in a cellular architecture thus enabling the system to perform basic image processing functions on the incoming image data. Thus hybrid architectures will allow integration of sensing and processing functions in ways analogous to biological systems.

Design Tools**:** Design tools are critical in developing new nanoarchitectures. Nanoscale devices need improved design methodologies and tools to cope with huge number of devices, large number of defects and transient faults.

The current CAD tools suite can't be scaled to handle systems with billions of components. In addition, they assume lower levels of defects and related faults and hence will not synthesize nanocircuits with required level of fault tolerance, error correction and detection and diagnosability. The level of design entry and abstraction must be raised from register-transfer level to the architecture and system level in order to manage design complexity due to huge number of nanodevices available.

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