STATISTICAL FAULT SIMULATION.

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ABSTRACT:

Fault simulation is used for the development or evaluation of manufacturing tests. However with the increase in the number of gates in the circuit, the number of faults increases proportionally resulting in high computational time for a complete fault simulation. The complexity is found to increase at least as the square of the number of gates and thus is exponential in nature. To overcome the high computational requirements, statistical sampling methods have been proposed. In fault sampling, a subset of the total faults known as fault sample is used for simulation. The fault coverage obtained in this simulation is then used to estimate the fault coverage of the complete fault list within a small error range. Since the fault sample is small compared to the actual fault set, the reduction in computation is great. The sample size is independent of the total number of faults covered and is determined by the accuracy in which the fault coverage is to be estimated.

In this paper, we conduct a study on statistical fault simulation looking at the various sampling schemes proposed and its applications. We also look briefly into the statistical theories behind the sampling techniques and do a comparative study of the results from different sampling algorithms.

1. INTRODUCTION.

Fault simulation is an essential method of determining the fault coverage provided by a given test set for a given VLSI circuit. However with the increase in complexity of modern day VLSI chips, the number of faults also increases proportionately and thus the time taken to conduct a exhaustive fault simulation has increased exponentially. The complexity of fault simulators is known to grow at least as the square of the number of gates in the circuit as experimentally shown in [1]. Despite methods like fault dropping, parallel, concurrent, deductive, differential fault simulation or the use of specialized fault simulation accelerators[2] , the simulation time is still quite high which is a serious limitation in the field of VLSI testing

Fault sampling was introduced to estimated the fault coverage of a given test vector at a fraction of the time taken by an exhaustive fault simulation. In this technique a subset of faults is randomly selected from the total number of faults to be simulated. This subset known as a *fault sample* is then used fault simulated to give an estimated fault coverage known as *sample coverage* [3]. From this sample coverage the actual fault coverage of the test vectors is estimated within a small error range. Since the fault sample is much smaller compared to the actual fault set, the simulation time taken is greatly reduced. The accuracy of the estimated fault coverage will depend of the size of the sample taken. A larger sample would give a more precise estimate. Thus the size of the sample is independent of the actual total number of faults, but is based on the accuracy by which the sample coverage is desired to be estimated.
The rest of this paper is organized as follows: Section 2. looks into the statistical theories behind sampling and how it is used in fault sampling. Section 3. involves a discussion of the various sampling techniques proposed in literature and its applications in fault simulation. Section 4. is a brief look into the results from some of the above mentioned sampling techniques. Section 5. concludes this paper.

2. THEORECTICAL BACKGROUND.

To understand the various the fault sampling applications, a brief look into the basics of statistical theory and how the sample coverage is an estimate for the true value coverage and the resulting coverage estimate.

Consider an event involving the flipping of a fair coin. If getting a head is a success and tails a failure, then the probability of getting a success is 0.5 and failure is 0.5 for one flip of a coin. For n such trials if we want k success the probability is given by

$$\text{P (k success in n trials)} = \binom{n}{k} p^k q^{n-k}$$

Here k is referred to as binomial random variable and the distribution of probabilities of possible outcomes is known as binomial distribution [9]. This applies any system in which each trial described by the probability distribution is independent of each other. Events of this kind is also known as sampling with replacement. If the trials are dependent on each other then probability of success or failure is changed with each trial. This also known as sampling with replacement and fault sampling is an experiment of this type. The probability of success is described by:

$$\text{P (k success in n trials)} = \frac{\binom{r}{k}\binom{w}{n-k}}{\binom{r+w}{n}}$$

where r is the number of possible successes and w the number of possible failures. Such kind of a distribution is known as hyper geometric distribution.

In fault sampling a success is defined as a fault detected and a failure is an undetected fault. Being a hyper geometric distribution, one can estimate the probability of the sample fault coverage i.e. the number of detected faults from the total number of sampled faults using notation adopted from [3]:

Np - actual total number of faults.

C - actual fault coverage (un known and to be estimated).

C Np - actual number of detected faults.

Ns - number of randomly sampled faults.

x - sample coverage determined from sample fault simulation

x Ns - number of sampled faults detected.

Thus from the above hyper geometric distribution we get:

$$\text{P (sample coverage)} = \frac{\binom{CNs}{xNs}\binom{(1-C)Np}{(1-x)Ns}}{\binom{Np}{Ns}}$$

If the probability density function is approximated to a Gaussian probability distribution then the true value coverage can be represented as the mean of the sample fault coverage, showing that the sample coverage is an unbiased estimate of the true coverage [3].

From [14], the three sigma range or the error bound is used to obtain the estimated coverage from the sample coverage which is approximated as in [3]:

$$3\sigma \text{ coverage estimate} = x \pm \frac{4.5}{Ns}\sqrt{(1+0.44\, N_S\, x(1-x)}$$

3. FAULT SIMULATION APPLICATIONS.

In this section we take a look in the literature at the various applications done in the statistical fault simulation area. In [4], Agrawal has divided fault sampling as : fixed size random sampling method and sequential fault sampling.In fixed – size random sampling proposed by Mcdermott [7] and Agrawal [4], a fault sample is randomly selected from the actual fault set and the size of the sample is determined based on the particular fault coverage estimate to be achieved within a specified error bound. It has been observed that as the sample size approaches 1000, the fault coverage approaches the true coverage for any circuit [4]. This is because the sample size is dependent on the desired confidence range for fault coverage estimate and not on the size of the circuit.

Sequential sampling involves the simulation of a number of smaller sampled fault sets (a multi pass sampling procedure), with each pass resulting a fault coverage estimate closer to actual fault coverage value. In the Agrawal approach a coverage range that bounds the estimated fault coverage can be determined as opposed to a similar work by Case [6] in which accept/reject test sets are used based on the number of faults detected/undetected by each fault sample used.

Stratified sampling as discussed in [9] attempt to reduce the error margin in random sampling even further. Basically, the sample space is divided into further sub spaces or called as *strata* such that all samples in particular strata share some common trait. Samples from each stratum are taken and the sum of the weighted estimations got from the various subspaces is used in the fault coverage. Here the dilemma is how to determine which faults go to which strata. This should be done such that the weighted sum of fault coverage estimations from each strata is closer the actual fault coverage estimate than the estimation got from simple random sampling. Various fault classification techniques has also been explored in [9].

Statistical Fault Analysis or STAFAN was proposed in [8] as an alternative method to fault simulation of digital circuits. Here detection of a fault is determined by calculating the control abilities and observabilities of circuit nodes. The probability of detecting a fault is computed using the probability of controlling an input node and the probability of observing the propagated value at the output node. Thus by using the calculated fault detection probabilities, the fault coverage can be estimated. Though it comes with a small overhead it has the advantage of using only fault free (true value) simulation with a complexity linear to the number of nodes.

In Thaker, Agrawal and Zaghloul paper [11], stratified fault sampling is used in RTL fault simulation to estimate the gate level coverage of test vectors. Each RTL module is simulated using RTL fault models and the resultant RTL fault list is used as a fault sample representing the stuck at fault set of that RTL module. The RTL coverage is experimentally shown in this paper to track the gate level coverage within statistical error bounds. The weighted sum of all the RTL modules like in stratified sampling is used to determine the overall RTL coverage.

Sampling techniques have also been used in test generation as proposed in [10]. In this technique the fault set is randomly divided into two groups. The smaller group called as the sample is used in fault simulators and test generators and the fault coverage is deterministically estimated. The coverage of the other group is done using random vectors and estimated from the fault detection probabilities of the circuit nodes. By increases the sample size would increase the number of test vectors and hence random coverage. Thus the technique attempts to find out the coverage got from random vectors and deterministic ones. A first pass test generation is done using a sample and from the coverage obtained from this random sample, a detection probability distribution is determined using Bayes' Theorem. From this the coverage of the unsampled group is also determined. A second pass may be done to get more accurate results. Fault sampling techniques also found application in sampling of test vectors and using these vectors samples for fault coverage as proposed in [12]. Using ideas similar to STAFAN, the test vector samples are used to calculate the controllability's and observability's of the circuit lines and then used in detection of faults and hence estimate fault coverage.

4. RESULTS FROM SAMPLING TECHNIQUES.

In the section we take a brief look at few results got from some of the above described statistical fault simulation and sampling techniques. In STAFAN [8], the fault coverage results for various circuits including 64 bit ALU and sequential circuits with over 1900 gates are shown in Table 1. From the fault coverage graph, Fig 1, it can be seen that the fault coverage estimation by STAFAN is quite close to the actual fault coverage using a fault simulator.

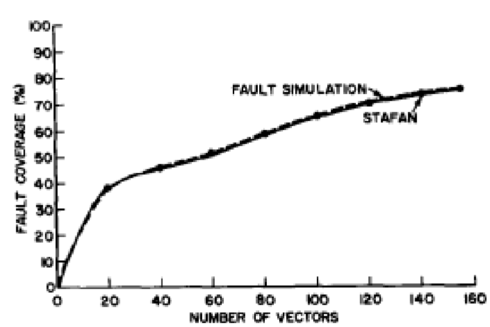

Fig 1: STAFAN fault coverage graph for 64 bit ALU

Circuit	# of vec.	# of faults	N	Final Coverage C	x	|err|
4-bit ALU	52	263	10	0.9657	0.9625	0.0047
64-bit ALU	155	4376	20	0.7530	0.7509	0.0029
4-bit Mult.	1111	741	100	0.9312	0.8680	0.0337
Circuit A	3842	5060	200	0.8644	0.8361	0.0124
Circuit B	3636	5856	200	0.7126	0.7257	0.0365

Table 1: STAFAN results. Here N is the number of test vectors , C is the true fault coverage, x is the estimated coverage and |err| is the deviation of x from the true coverage C.

Table 1 — Test generation by fault sampling

Sample Size	Circuit Name →	C2670	C6288	C7552
	Total Faults →	2747	7744	7550
500	Vectors →	71	25	81
	Sample Cov. (%) →	99.4	100.0	99.2
	Estimated Cov. (%) →	94.5	97.2	93.3
	Measured Cov. (%) →	–	98.3	–
	Total CPU Sec. →	3246	36	1180
	Fault Sim. CPU Sec. →	13	13	42
1000	Vectors →	96		
	Sample Cov. (%) →	99.4		
	Estimated Cov. (%) →	96.8		
	Measured Cov.(%) →	97.3		
	Total CPU Sec. →	3966		
	Fault Sim. CPU Sec. →	18		
1500	Vectors →			149
	Sample Cov. (%) →			99.4
	Estimated Cov. (%) →			96.6
	Measured Cov. (%) →			96.5
	Total CPU Sec. →			5749
	Fault Sim. CPU Sec. →			79
All Faults	Vectors →	149	38	297
	Coverage (%) →	100.0	100.0	99.7
	Redundant Faults →	117	34	131
	Total CPU Seconds →	17186	110	33806
	Fault Sim. CPU Seconds →	32	52	174

Table 2. Test generation results using fault sampling.

SA2901 WITH PARTITIONING METHOD

Sample size	Fault Coverage Estimate (± 5%)	Estimate Variance
All faults	99.0%	0
385	99.3%	0.00002
385	98.6%	0.00004
385	98.4%	0.00004
385	99.3%	0.00002
	mean fault coverage estimate -- 98.9% standard deviation -- 0.41	
663	99.3%	0.00001
663	98.9%	0.00002
663	98.9%	0.00002
663	99.1%	0.00001
	mean fault coverage estimate -- 99.05% standard deviation -- 0.17	

Table 3. Simple Random Sampling results

SA2901 WITH BEST BIST METHOD AND STRATIFIED SAMPLING USING RANDOM STRATA CLASSIFICATION

Sample size	# of Strata	Weighted Fault Coverage Estimate	Weighted Estimate Variance
All faults	1	54.6%	0
663	3	55.1%	0.00037
663	3	54.2%	0.00037
663	3	57.1%	0.00037
663	3	57.1%	0.00037
	mean fault coverage estimate -- 55.9% standard deviation -- 1.27		

Table 4. Stratified Random Sampling results.

Test generations results using fault sampling [10] are given in Table 2. The results are shown are obtained from two test passes, the first with sample size 500 and the second with sizes 1000 and 1500 respectively. Tables 3. and 4. show the results of simple random sampling and stratified random sampling respectively as published by paper [9]. The sampling experiments were done using Sandia SA2901 with BIST circuitry and a test set of 10000 LFSR (linear feed back shift register) generated input patterns. Table 3 depicts results using two fixed samples of 365 and 663 faults drawn (without replacement) while Table

4. results are from a similar experiment with a total fault set of 1339 faults partitioned into3 stratum of equal size as explained in [9].

4. CONCLUSION.

A study of statistical fault simulation was conducted in this paper. Statistical theories involved in fault sampling and the various fault sampling algorithms and applications haven been explored and discussed. Few results from different sampling algorithms in the literature have been given. From the above discussion it can be concluded that in the present day scenario, fault sampling and statistical fault simulation have been a much needed solution for reducing high fault simulation computational time. The use of these fault sampling ideas in test vector generation [10] and sampling [11] shows much promise with the ever increasing number of test vectors in the testing of VLSI circuits.

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