

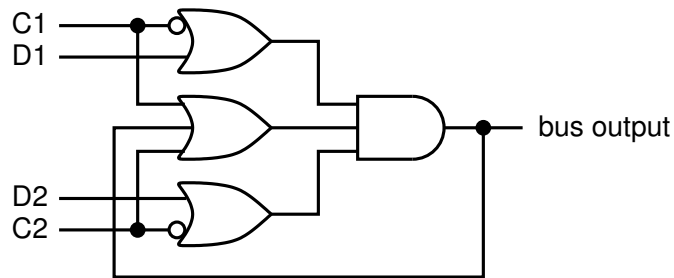
Solutions to Homework 4 Problems

ELEC 7250 VLSI Testing (Spring 2006)

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Problem 5.8

The following schematic shows a logic model for a bus with memory. When both drivers feed data to the bus, i.e., $C1 = C2 = 1$, $D1 \cdot D2$ appears at the output, assuming a 0-dominance. When both drivers are turned off, i.e., $C1 = C2 = 0$, the output retains its value through feedback. When only one driver is on, the corresponding data input appears at the output.



This model represents most of the characteristics of a MOS bus, with the exception of bidirectionality. One problem with it is that it is an asynchronous sequential circuit and cannot be correctly simulated by some simulators. An event-driven logic simulator can simulate it, but will be inefficient in comparison with synchronous circuit simulation.

Problem 5.16

Since no fault dropping is used, the serial fault simulator must simulate the entire circuit $n + 1$ times. Assuming the CPU time for one simulation with all vectors is t , total time of serial fault simulation is given by,

$$T(\text{serial}) = t(n + 1)$$

Using CPU time t , the parallel simulator processes $w - 1$ faults. Thus, it will make $n/(w - 1)$ such passes, requiring total time,

$$T(\textit{parallel}) = \frac{tn}{w - 1}$$

Therefore,

$$\frac{T(\textit{serial})}{T(\textit{parallel})} = \frac{(n + 1)(w - 1)}{n}$$