

Solutions to Homework 3 Problems ELEC 7250 VLSI Testing (Spring 2006)

February 9, 2006

Problem 4.7 Fault indistinguishability

Without loss of information we will write a function $f(V)$ as f . Thus, the left hand side of Equation 4.3 is:

$$\begin{aligned}
 & [f_0 \oplus f_1] \oplus [f_0 \oplus f_2] \\
 &= [f_0 \overline{f_1} + \overline{f_0} f_1] \oplus [f_0 \overline{f_2} + \overline{f_0} f_2] \\
 &= (f_0 \overline{f_1} + \overline{f_0} f_1) \overline{(f_0 \overline{f_2} + \overline{f_0} f_2)} + \overline{(f_0 \overline{f_1} + \overline{f_0} f_1)} (f_0 \overline{f_2} + \overline{f_0} f_2) \\
 &= (f_0 \overline{f_1} + \overline{f_0} f_1) \overline{(f_0 \overline{f_2} + \overline{f_0} f_2)} + (f_0 \overline{f_1} + \overline{f_0} f_1) (f_0 \overline{f_2} + \overline{f_0} f_2) \\
 &= (f_0 \overline{f_1} + \overline{f_0} f_1) (\overline{f_0} + f_2) (\overline{f_0} + \overline{f_2}) + (\overline{f_0} + f_1) (\overline{f_0} + f_2) (f_0 \overline{f_2} + \overline{f_0} f_2) \\
 &= (f_0 \overline{f_1} + \overline{f_0} f_1) (\overline{f_0} \overline{f_2} + \overline{f_0} f_2) + (\overline{f_0} + f_1) (\overline{f_0} + f_2) (f_0 \overline{f_2} + \overline{f_0} f_2) \\
 &= f_0 \overline{f_1} f_2 + \overline{f_0} f_1 \overline{f_2} + \overline{f_0} \overline{f_1} f_2 + f_0 f_1 \overline{f_2} \\
 &= (\overline{f_1} f_2) (\overline{f_0} + \overline{f_0}) + f_1 \overline{f_2} (\overline{f_0} + f_0) \\
 &= \overline{f_1} f_2 + f_1 \overline{f_2} \\
 &= f_1 \oplus f_2 \\
 &= \text{Left hand side of Equation 4.4}
 \end{aligned}$$

This completes the derivation of Equation 4.4 from Equation 4.3.

Problem 4.8 Functional equivalence

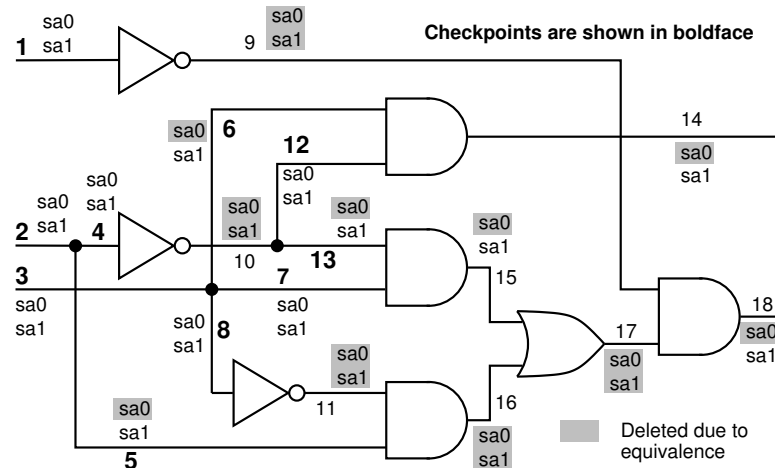
Faulty functions for the circuit of Figure 4.12 corresponding to the two faults are:

$$\begin{aligned}
 i(c \ s - a - 0) &= b(\overline{ab}) = \overline{ab} \\
 i(f \ s - a - 1) &= (a + b)\overline{a} = \overline{ab}
 \end{aligned}$$

The two faulty functions are indistinguishable and hence **the two faults are equivalent.**

Problem 4.11 Equivalence and dominance fault collapsing

- (a) The given circuit is shown below with fault sites marked by numbers. The number of potential fault sites is 18. The total number of faults is 36.



Circuit for Problem 4.11: (b) Equivalence collapse ratio = $20/36 = 0.56$
(c) Dominance (uncollapsed faults at checkpoints) collapse ratio = $17/36 = 0.47$

- (b) The figure shows deletion of equivalent faults using an output to input pass. Of the 36 faults, 20 remain, giving a collapse ratio $20/36 = 0.56$.
- (c) Checkpoint lines are shown by boldface numbers. These are three PIs and seven fanout branches. Line 2 fans out to 4 and 5. Line 3 fans out to 6, 7 and 8. Line 10 fans out to 12 and 13. There are ten checkpoints and 20 checkpoint faults. Further, s-a-0 faults on lines 6 and 12 are equivalent and any one of them can be chosen. Similarly, s-a-0 faults on 7 and 13 are equivalent, and so are s-a-0 on 5 and s-a-1 on 8. Thus, the size of the fault set is reduced to 17, giving a collapse ratio $17/36 = 0.47$.