Solutions to Homework 1 Problems
ELEC 7250 VLSI Testing (Spring 2006)

January 30, 2006

Problem 1.1 Chip testing

Let x denote the escape probability, $Prob(P|FQ)$. Referring to the formula derived in Problem 1.1, a defect level of 500 *ppm* means,

$$\frac{Prob(P|FQ)Prob(FQ)}{Prob(P)} = \frac{x \times 0.3}{0.95 \times 0.7 + x \times 0.3} = 0.0005$$

This gives,

$$x = \frac{0.0003325}{0.29985}$$

Next, we obtain,

$$\begin{aligned} \text{Defect coverage} &= Prob(F|FQ) = 1 - Prob(P|FQ) \\ &= 1 - x = 0.99889 \end{aligned}$$

The required defect coverage is 99.889%. This represents the capability of the test in detecting the actual "defects" that occur and should not be confused with the "fault coverage," which is defined for the "single stuck-at" fault model.

Problem 1.4 Test cost and self-test

Following Example 1.2 of the book (pp. 10-11), we obtain

$$\text{ATE purchase price} = \$1.2M + 256 \times \$3,000 = \$1.968M$$

Assuming a 20% per year linear rate of depreciation, a maintenance cost of 2% of the price, and an annual operating cost of $\$0.5M$,

$$\text{Running cost} = \$1.968M \times 0.2 + \$1.968M \times 0.02 + \$0.5M = \$932,960/year$$

$$\text{Testing cost} = \frac{\$932,960}{365 \times 24 \times 3600} = 2.96\ cents/second$$

Testing cost of the self-test design is 2.96 cents per second, down from 4.56 cents per second calculated in Example 1.2