

Solutions to Homework 10 Problems

ELEC 7250 VLSI Testing (Spring 2006)

April 29, 2006

Problem 13.1 Leakage fault tests

Examining Figure 13.12(c), we see that rows $i = 1, 2,$ and 4 of the leakage fault table cover all possible tests. We need these stuck-fault vectors:

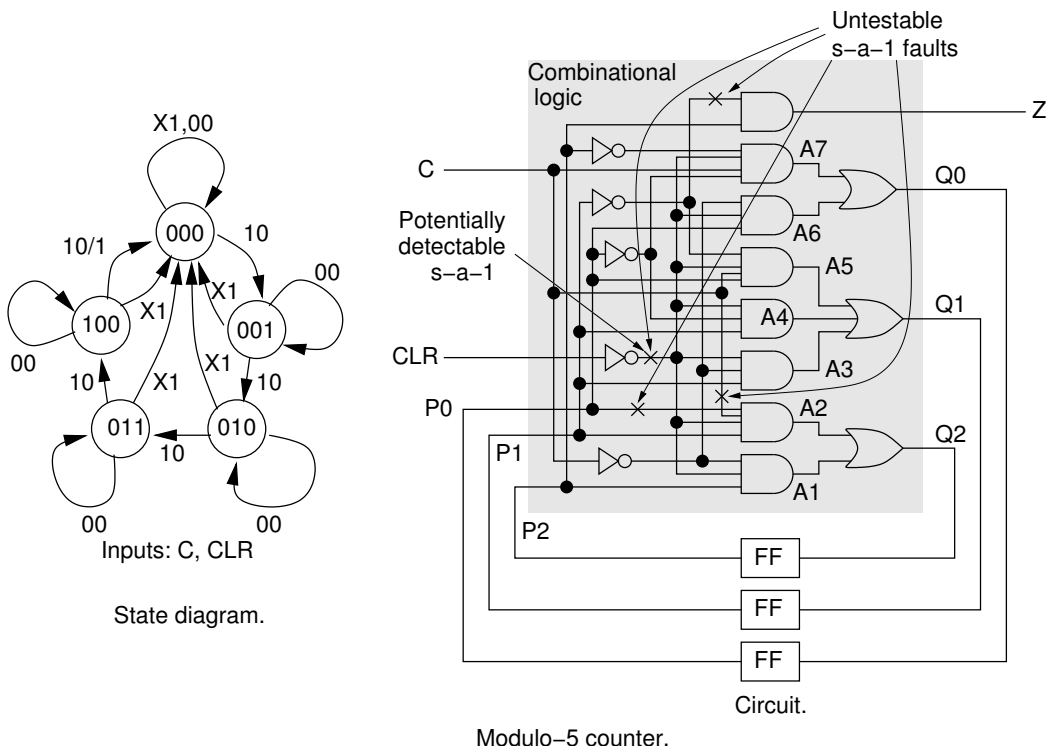
I_1	I_2	O_1	
0	0	1	$i = 1$
0	1	0	$i = 2$
1	0	0	$i = 4$

Problem 14.5 Modulo-5 counter circuit

The following figure shows a modulo-5 counter circuit. As shown in the state diagram, the states are encoded as 000, 001, 010, 011 and 100. The input $CLR = 1$ initializes the circuit to the 000 state. Input $C = 1, CLR = 0$ advances the state at every clock. The clock signal applied to the three D flip-flops is not shown.

The output Z remains 0 with the exception of the state 100, which produces a $Z = 1$ output.

The combinational circuit (shown in the grey box) is made completely single-fault testable by removing redundant faults that were identified by an ATPG program.



For the sequential counter, a sequential circuit ATPG program produced 62 vectors to obtain a coverage of $(57/62) \times 100 = 92.98\%$. The five untestable faults were all s-a-1 type and are shown in the figure. Among these the s-a-1 fault on the *CLR* signal was potentially detected by the test set.

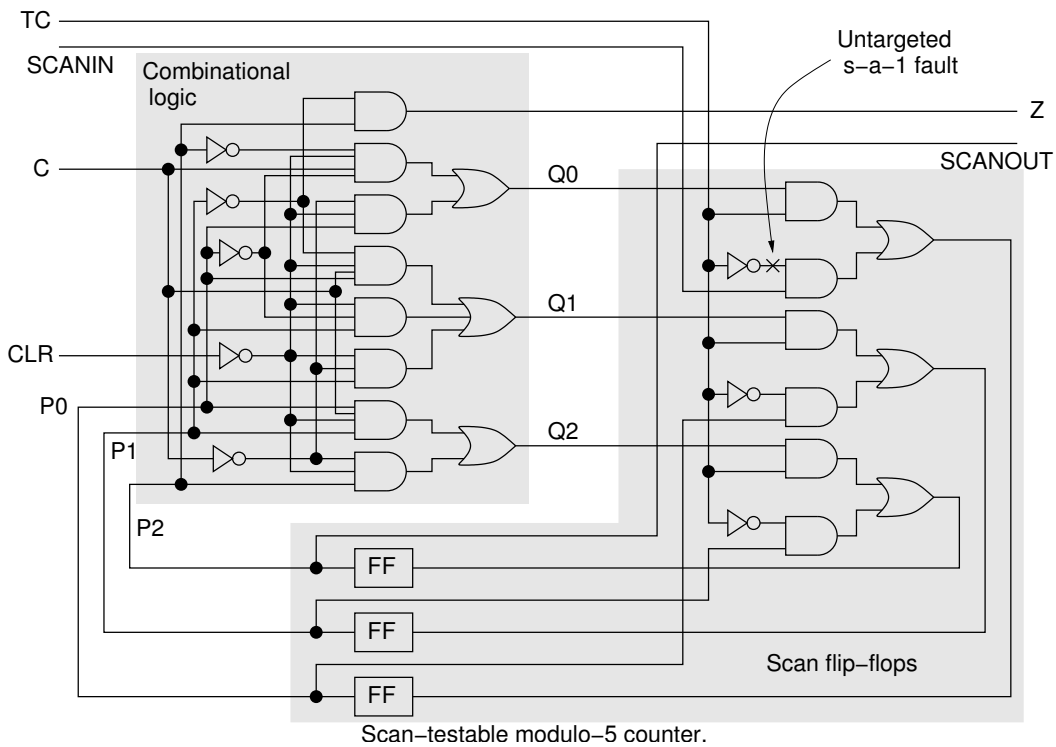
Problem 14.6 Full-scan design

The following figure shows the scan design of the modulo-5 counter.

The number of vectors obtained may vary depending on the ATPG program used. These results were obtained from Bell Labs' Gentest program. The combinational circuit, whose inputs are *C*, *CLR*, *P0*, *P1* and *P2*, and outputs are *Z*, *Q0*, *Q1* and *Q2*, has a collapsed set of 57 faults. All of these faults were detected by 16 vectors.

A complete scan sequence consists of 74 vectors (see Equation 14.1 in the book), which includes 7 vectors for testing the scan register. The scan circuit contains a collapsed set of 79 faults. Fault simulation of the 74-vector sequence showed that 78 faults were detected. The undetected s-a-1 fault is marked on the circuit diagram. It is at the output of the test control (*TC*) inverter in the first multiplexer.

The reason this fault is not detected is that it was never targeted. Since the scan register test holds *TC* to 0 for a continuous scan mode, this fault was not activated. The fault is, however, activated every time the circuit is set in the normal mode during the application of the scan sequence. Since in the normal mode the state of *SCANIN* is considered irrelevant, *SCANIN* was arbitrarily set to 0. That



prevented the propagation of the fault effect. A suitable strategy for detecting this fault is to set $Q0$ outputs of the combinational logic as 0 by applying $CLR = 1$. At the same time, the circuit is set in the normal mode by applying $TC = 1$. The fault effect is now propagated to the flip-flop and can be scanned out.

We notice that similar faults in the other two multiplexers were detected by our scan sequence. This is due to the chance occurrence of normal data as 0 and scan data as 1 when $TC = 1$, which would place the fault effect in the flip-flop. $TC = 1$ was always followed by scanout that detected the fault.

In general, it can be recommended that $SCANIN$ is set to 1 whenever the circuit goes to the normal mode ($TC=1$), provided the AND-OR type of multiplexer is used.

Problem 15.17 Fault detection

ABC	Good $R_1R_2R_3$	C s-a-0		C s-a-1		$C - g$ s-a-0	
		YZ	Bad $R_1R_2R_3$	YZ	Bad $R_1R_2R_3$	YZ	Bad $R_1R_2R_3$
001	000	10	000	11	000	10	000
100	011	10	010	11	011	10	010
010	011	10	111	01	010	10	111
101	011	10	001	11	100	10	001
110	010	10	110	11	001	10	110
111	111	10	101	11	111	10	101
011	000	10	100	01	000	01	100
001	001	10	000	11	001	10	011
	111		010 Yes		111 No		011 Yes

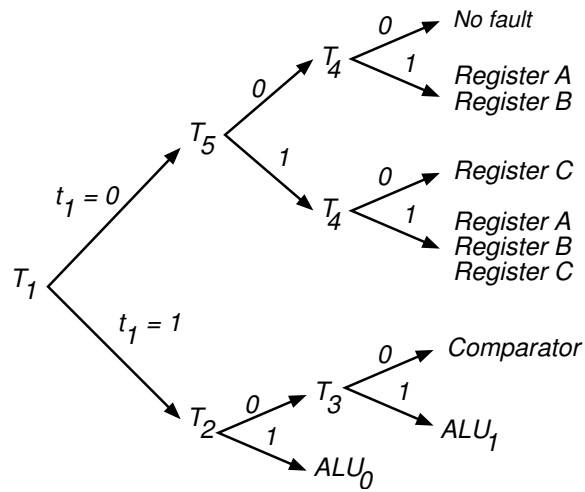
ABC	Good $R_1R_2R_3$	$C - g$ s-a-1		$f - Y$ s-a-0		$f - Y$ s-a-1	
		YZ	Bad $R_1R_2R_3$	YZ	Bad $R_1R_2R_3$	YZ	Bad $R_1R_2R_3$
001	000	11	000	00	000	10	000
100	011	11	011	00	000	10	010
010	011	11	010	00	000	10	111
101	011	11	110	01	000	11	001
110	010	11	100	00	001	10	111
111	111	11	001	01	100	11	001
011	000	01	111	01	011	11	111
001	001	11	010	01	000	11	000
	111		110 Yes		001 Yes		011 Yes

Problem 18.7 Diagnosis

A diagnosis tree for the system of Figure 18.4 and its tests shown in Table 18.3 is shown below.

We first apply test T_1 . If it fails, i.e., $t_1 = 1$, we presume that either the ALU's or the comparator are faulty. So, we apply T_2 . A failure now means $ALU0$ is faulty. Otherwise, we apply T_3 , which either fails if $ALU1$ is faulty, or passes if the comparator is faulty.

If T_1 passes, we assume that ALU's are not faulty and the x 's is the syndromes of ALU's under t_4 and t_5 can be changed to 0. Also, the rest of the procedure assumes that only one unit is faulty. We apply T_5 followed by T_4 . If T_5 fails and T_4 passes then *Register C* is considered faulty. If T_5 passes and T_4 fails then both *Register A*



and *Register B* become suspects. If both tests fail then we conclude that perhaps *Register C* and at least one among the other two registers are faulty.

The diagnostic tree shows that the procedure terminates with the application of three or fewer tests.