# Defect-level and Fault Coverage

*(ELEC 7250 Term paper)*
*Gefu Xu*
*Reviewer: Weidong tang*

***1.Abstract***

In the paper, the concepts of defect-level and fault coverage are discussed. The definition and examples of defect-level and fault coverage are showed in part 3 and part 4 to clarify these two terms. At the end of the paper, we summarize the defect-level and fault coverage and draw the conclusion.

***2.Introduction***

VLSI yield and quality measured as defect-level and fault coverage are important concepts related to electronic production and testing. [1] Both of defect-level and fault coverage are wildly used in today's test field. For VLSI chips, it's necessary for manufacturer to make the tradeoff between the test cost and high fault coverage. Some defect chips will be shipped to the market in terms of this kind of tradeoff. Therefore, using defect-level to specify the quality is important and needed.

***3.Defect-level (DL)***

***Definition***

Defect-level (DL) is the fraction of faulty chips among the chips that pass the test, expressed as parts per million (ppm). [1]

For VLSI chips, while a defect level of 500 ppm may be acceptable, 10 ppm or lower represents high quality.

***Measurement***

There are two ways to measure the defect-level. One is to consider the number of returned chips from market and the other is to analyze the test data during the test process.

One way to measure the defect level is to gather the data from the field return.

After VLSI chips leave the manufacturing facility, they may fail and be returned to the manufacturer for the following reasons:

*Failing acceptance test.* The customer conducts an acceptance test on the parts before they are mounted on printed circuit boards. If a part fails the test it is returned to the supplier. [1]

*Failing system test.* A board fails the system test but passed when one or more chips are replaced. The removed chips are returned to the chip supplier. [1]

*Failing maintenance test.* A maintenance test is conducted on a system operating in the field for both regular maintenance and diagnosis when an operational failure occurs. The faulty part is located and replaced. While the system goes back to operation, the replaced board is returned to a repair shop, where faulty chips are found and replaced. The faulty chips are returned to the chip supplier. [1]

The number of these returned chips normalized to one million chips shipped is called Defect-level.

The other way to measure the defect level is to analyze test data from the test process. In this method, fault coverage of tests and chip fallout rate are analyzed and a modified yield model is fitted to the fallout data to estimate the Defect-level.

We can use follow equations 1) & 2) to calculate the Defect-level.

1) $$DL(T) = \frac{Y(T) - Y(1)}{Y(T)}$$ [2]

Where T is the fault coverage of tests, Y(T) is the measured yield with fault coverage T is applied, Y(1) is the measured yield when all faults are tested. For example, if the yield with fault coverage 95% is 90%, the yield with fault coverage 100% is 80%, then defect-level at fault coverage 95% is $\frac{0.9-0.8}{0.9}\times 100\% = 11.11\%$.

2) $DL(T) = 1 - \frac{(\beta + TAf)^{\beta}}{(\beta + Af)^{\beta}}$ [2]

Where T is the fault coverage of tests, $\beta$ is the fault clustering parameter, Af is the average number of faults on the chip of area A. Af and $\beta$ are determined by test data analysis.

## 4.Fault coverage (FC)

### Definition

Fault coverage is the ratio of detected faults to total faults. For example, if the total faults in a circuit are 200 and 143 faults are tested. Then the fault coverage of this circuit is $\frac{143}{200}\times 100\% = 71.5\%$.

### Fault coverage in VLSI test

Fault coverage is a very important concept in VLSI test. We usually use fault coverage to evaluate the efficiency of the test. We can measure the efficiency of different test structures, different test algorithms and different test strategys in terms of fault coverage.

People usually intend to pursue high fault coverage to achieve high chip quantity. In general, the coverage of combinational circuit is high and the coverage of sequential circuit is low. To improve the fault coverage of the sequential circuit, many efforts were made such as using scan method to change sequential circuit into combinational circuit to enhance the fault coverage.

Fault coverage is also a concept related with the test type. Different test may induce different fault set which will result in different fault coverage of the same circuit. For instance, the fault coverage of a circuit under stuck-at fault test, delay test and $I_{DDQ}$ test are totally different.

### Fault coverage and Fault efficiency

The difference between fault coverage and fault efficiency is shown as follows:

4) Fault coverage = number of detected faults / total number of faults

5) Fault efficiency = number of detected faults / number of detectable faults

6) Total number of faults = number of detectable faults + number of undetectable faults.

For example, the total faults in a circuit are 200, and 35 faults are undetectable and 143 faults are tested. Then the fault coverage of this circuit is $\frac{143}{200}\times 100\% = 71.5\%$ and the fault efficiency of the circuit is $\frac{143}{200-35}\times 100\% = 86.67\%$.

From the equations 4) 5) 6) and the example, we find that fault coverage and fault efficiency are related but have small difference.

## 5.Conclusion

In the paper, we introduce the concepts of defect-level and fault coverage which are very important in the VLSI test. Defect-level and fault coverage are both used to estimate the product quality. The equation 2) in part 3 reveals the relationship between the defect-level and fault coverage. Some examples are also used in the paper to clarify the defect-level and fault coverage.

## *6.References*

[1] Bushnell M.L. and Agrawal V.D., *Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits*, Kluwer Academic Publishers, 2000

[2] Agrawal & Bushnell, *VLSI test lecture*, 2001