

## Boundary Scan Standard

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**Abstract**— Boundary scan, or IEEE Standard 1149.1, is a standardized specification for providing a test access port and board test architecture directly within silicon chips. The standard describes how boundary-scan-compliant integrated circuits function, and how these devices are connected in a serial boundary-scan chain on a printed-circuit board. With boundary scan, solder faults and other structural, manufacturing problems can be identified without direct bed-of-nails access to every net on the board and without developing complex libraries to functionally test ICs. Boundary-scan tests can be administered using benchtop instruments as well as through high-volume in-circuit test systems. In this paper the concept of boundary scan standard is discussed. The summary of IEEE Boundary Scan Standard (IEEE 1149.1-2001) is given.

**Keywords:** — boundary scan, boundary-scan architecture, Boundary-Scan Description Language, boundary-scan register, circuit boards, circuitry, integrated circuit, printed circuit boards, TAP, test, test access port

### I. INTRODUCTION

IN THE 1970s, the *in-circuit testing* (ICT) method appeared, in which printed circuit boards (PCBs) are tested by probing the backs of the boards with nails. The component technology of that era was *dual in-line* (DIP) packages, which were attached to a PCB by drilling two rows of holes, inserting the DIP into the holes, and wave soldering the leads to the hole (or via), which was plated on the inside with metal. This testing mechanism relies on *nails* in a *bed-of-nails* tester. The nails are positioned to hit various solder bumps on the back of the PCB and they force various signal values on the component inputs, and measure the component output signals at various other solder bumps. With *Surface-mount technology* (SMT) which replaced dual in-line packages, components are now soldered onto a single side of the PCB without drilling holes in the PCB. There are no through-hole pin targets with solder bumps for nails to hit for SMT technology. And, some signals, which may never appear on the bottom side of a PCB, are simply unavailable for in-circuit testing.

SMT technology is not necessary obstacle for in-circuit tester nails if special test pins are provided. All of this resulted in the need to replace the PCB test delivery system to the component.

IEEE Standard 1149.1-2001 defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The facilities defined by the standard seek to provide a solution to the problem of testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high density surface-mounting assembly techniques. They also provide a means of accessing and controlling design-for-test features built into the digital integrated circuits themselves. Such

features might, for example, include internal scan paths and self-test functions as well as other features intended to support service applications in the assembled product.

### II. BOUNDARY SCAN ARCHITECTURE

#### A. System Configuration

Figure 1 shows an integrated circuit that complies IEEE Std. 1149.1 boundary scan standard. The IEEE 1149.1 boundary scan standard circuitry is comprised of 3 functional blocks: a test access port (TAP), a TAP controller and a set of registers. The meanings of signals in this figure will be detailed later.

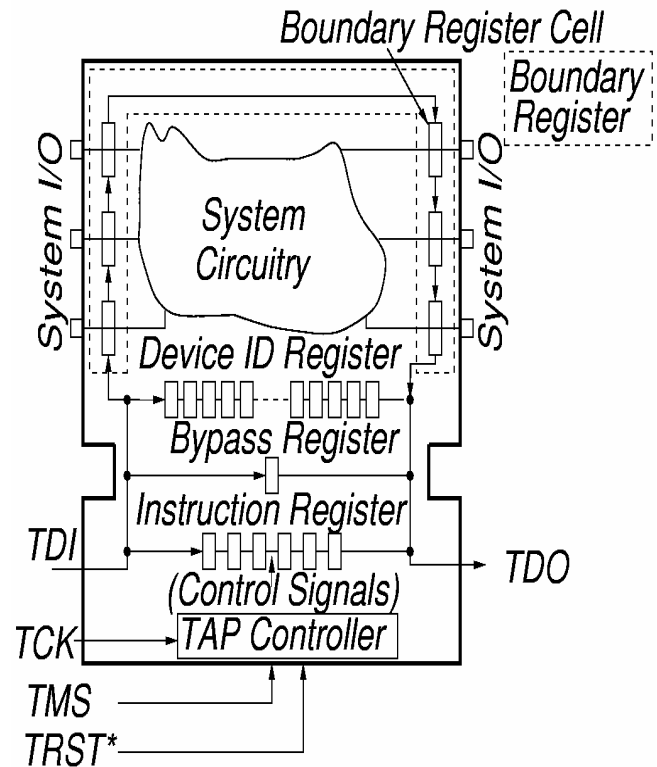
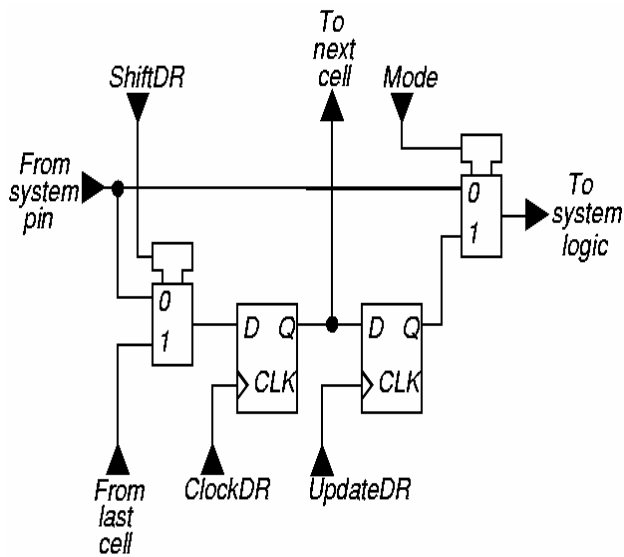


Figure 1 Schematic of System Test Logic

#### B. Boundary Register

The serial connection of these registers around the periphery of the chip at the pin is known as the boundary registers. Figure 2 illustrates an example implementation for a boundary-scan register cell that could be used for an input or output connection to an integrated circuit. Dependent on the control signals applied to the multiplexers, data can be either loaded into the scan register from the pin of “from system” or driven into the register through the “To system logic”. of the cell (e.g., into the core of the component design). The second flip-flop (controlled by input clock UpdateDR) is provided to ensure that the signals driven out

of the cell in the latter case are held while new data is shifted into the cell using input clock ClockDR.



**Figure 2 A Boundary Scan Register Cell**

The INSTRUCTION register permits specific commands to be shifted into the design to select a particular test data register and/or a specific test function. Additionally, the capture sequence of the INSTRUCTION register permits design specific data to be examined.

The INSTRUCTION register must be at least two bits long, and the two least significant bits must capture the value "01". The significance of the two bit minimum length is two fold. First it permits the ability to supply unique codes for at least each of the three mandatory instructions required by the standard. Secondly, the bit value "01" in the least significant locations can be used to check the connectivity of the scan chain by forcing a bit toggle at each instruction during a scan of the INSTRUCTION registers. This technique not only assists in determining the correct connectivity of the scan chain about the board, but also assists in pin-pointing the location of any break in the scan chain.

### C. Test Access Port (TAP)

The Test Access Port (TAP) consists of four pins dedicated solely to the operation of the test logic. The four pins include TMS (Test Mode Select), TDI (Test Data In), TDO (Test Data Out), and TCK (Test Clock). These products contain a power-up reset function in lieu of adding the TRST pin. The motivation of this option is to save package size and hence customer board space, thus making the decision to implement 1149.1 less costly to the system designer.

**TCK:** This input provides the test clock for the test logic defined by the IEEE 1149.1 Standard. In accordance with the standard requirements, all test logic will retain its state indefinitely upon stopping TCK at a logic low, or 0. Additionally, the same retention may occur upon stopping TCK at a logic high, or 1, which is a permission granted by the standard. The motivation for TCK to be a dedicated test input is 1) to insure that it can be used independently of system clocks running at different frequencies, 2) that it permits shifting of test data without altering any system logic state when undertaking on-line system monitoring tasks, and 3) that it can be used to test all board

interconnect even when that interconnect transfers clock signals from one device to another.

**TMS:** This input is the command signal to control system operation modes. Its value is accepted into the test logic upon the rising edge of TCK. This input has a pull-up resistor to implement a logic high for an undriven input. The requirement that an unforced TMS input produce a logic high is to ensure that the normal operation of the design can continue without interference from the test logic by guaranteeing that an undriven TMS input can put the TAP Controller into the Test Logic Reset state.

**TDI:** This signal provides the serial data input of test instructions and data to the test logic. Its value is accepted into the test logic upon the rising edge of TCK. This input has a pullup resistor to implement a logic high for an undriven input. Test data will arrive at TDO without inversion after the appropriate number of clock cycles as determined by the length of the register currently connected between TDI and TDO. The requirement that an unforced TDI input produce a logic high is to assist in the determination of manufacturing defects in the test scan chain interconnect. A consistent field of 1's in shifting out the data registers can indicate where a break in the scan chain interconnect occurred.

**TDO:** This signal provides the serial data output of test instructions and data from the test logic. Changes in the logic state and drive activity for this output occur upon the falling edge of TCK. This is to avoid a race condition when TDO is connected to TDI of the next chip in the scan chain which is sampled on the rising edge. This output shall remain inactive except when the scanning of data is in progress. This is to permit the ability to multiplex scan chains on the board without causing signal contention between multiple TDO outputs connected together to form parallel scan chains.

### D. TAP Controller

TAP controller is a 16 state finite state machine which controls the insertion of the data and instruction registers (described later in this document) between TDI and TDO pins, and controls the flow of data through these registers. Changes in the state of the TAP Controller are solely a response to the value of TMS upon the rising edge of TCK, or upon power-up (or the application of a logic low to the optional TRST input which is not included in the products referring to this document). In any given state actions of the test logic taken in that state occur on the falling or rising edge of TCK following the rising edge of TCK which caused the TAP Controller to enter the state initially. The TAP controller must adhere to the standard state diagram shown in Figure 3.

**Test Logic Reset:** In this state, the boundary scan test logic is disabled to allow the device to function normally. All boundary scan registers are reset to their default states. This state is entered by at most, five TCK cycles while holding TMS high or asynchronously by pulling TRST low (if TRST pin is included). The IEEE 1149.1 standard requires that an internal pull-up be included on the TMS pin to assure the TAP will return and remain in test logic reset if TMS is floating.

**Run Test/Idle:** This state provides a dual purpose depending on the active instruction. It is included to allow for optional or user defined tests, including BIST, to be performed. For the required IEEE 1149.1 instructions, all test data registers retain

their current state (i.e., remain idle).

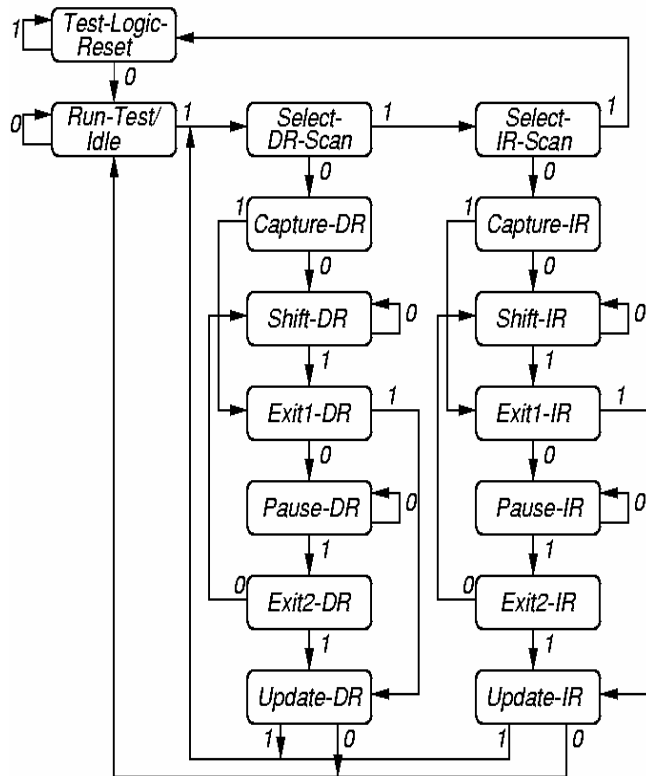


Figure 3 TAP Controller State Diagram

**SELECT-DR Scan:** This is a temporary state in which all test data registers retain their previous values.

**Capture-DR:** In this controller state data may be parallel loaded into the data register selected by the current instruction; otherwise, it retains its previous values.

**SHIFT-DR:** In this state the test data register selected between TDI and TDO by the current instruction will shift one stage at each rising edge of TCK. TDO is active during this state. Test data registers not selected by the current instruction maintain their previous values.

**Exit1-DR:** This is a temporary state in which all test data registers retain their previous values.

**PAUSE-DR:** This is a temporary state in which all data registers retain their previous values. This state is intended to temporarily halt the shifting of test data into the data register selected while retaining the ability to keep TCK running; TCK may be a free-running clock. This state is often used to load additional test vectors from external memory.

**Exit2-DR:** This is a temporary state in which all test data registers retain their previous values.

**UPDATE-DR:** The parallel output register of the selected test data register may be updated on the falling edge of TCK in this state, provided the test data register has such a parallel output register. The intent of the parallel output register is to provide the ability to apply the contents of the test data registers to the test logic simultaneously rather than applying it as it is being shifted in. All test data registers not selected by the current instruction retain their previous values.

**SELECT-IR Scan:** This is a temporary state in which the INSTRUCTION register retains its previous value.

**Capture-IR:** In this controller state, a fixed value must be parallel loaded into the INSTRUCTION register. The only restriction on what that data may be is that its least significant bit must be a logic high, or 1, and its second least significant bit must be a logic low, or 0. These opposite state bits can be used to check the correct operation of the scan chain on the board by forcing a bit toggle when the instructions are shifted.

**SHIFT-IR:** In this state the INSTRUCTION register selected between TDI and TDO will shift one stage at each rising edge of TCK. TDO is active during this state.

**Exit1-IR:** This is a temporary state in which the INSTRUCTION register retains its previous value.

**PAUSE-IR:** This is a temporary state in which the INSTRUCTION register retains its previous value. This state is intended to temporarily halt the shifting of test data into the INSTRUCTION register while retaining the ability to keep TCK running. This state is often used to load additional test vectors from external memory.

**Exit2-IR:** This is a temporary state in which the INSTRUCTION register retains its previous value.

**UPDATE-IR:** The parallel output register of the INSTRUCTION register will be updated on the falling edge of TCK in this state. The intent of the parallel output register is to provide the ability to apply the contents of the INSTRUCTION register to the test logic simultaneously rather than applying it as it is being shifted in.

#### E. Boundary Scan Test Instructions

We now simply describe the various JTAG TAP Controller test instructions.

**SAMPLE/PRELOAD:** This instruction allows a "snapshot" of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the Boundary-Scan SHIFT register prior to selection of another Boundary-Scan test instruction. During this instruction the Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state. When this instruction is selected, the states of all signals on the system pins will be loaded into the Boundary-Scan register upon the rising edge of TCK in the CAPTURE-DR state and the contents of the Boundary-Scan register will be loaded into the parallel output register included with the Boundary-Scan register bits upon the falling edge of TCK in the UPDATE-DR state.

**EXTEST:** This instruction allows circuitry external to the component package, typically the board interconnect, to be tested. Boundary-Scan register cells at the output pins are used to apply test stimuli, while those at the input pins capture test results. When this instruction is selected, the states of all signals on the system input pins will be loaded into the Boundary-Scan register upon the rising edge of TCK in the Capture-DR state and the contents of the Boundary-Scan register will solely define the state of the system outputs upon the falling edge of TCK in the UPDATE-DR state. This instruction is mandatory under the guidelines of IEEE Standard 1149.1. The 000. . . 0 instruction binary code must invoke the EXTEST instruction. During this instruction the Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state. Additional binary codes for this instruction are permitted.

**INTEST:** The optional INTEST instruction is one of two instructions defined by this standard that allow testing of the on-chip system logic while the component is assembled on the board. Using the INTEST instruction, test stimuli are shifted in one at a time and applied to the on-chip system logic. The test results are captured into the boundary-scan register and are examined by subsequent shifting. Data typically would be loaded onto the latched parallel outputs of boundary-scan shift-register stages using the PRELOAD instruction before selection of the INTEST instruction.

**RUNBIST:** The optional instruction causes execution of a self-contained self-test of the component. Use of the instruction allows a component user to determine the health of the component without the need to load complex data patterns and without the need for single-step operation (as required for the INTEST instruction). While the RUNBIST instruction is selected, the state of all system output pins is determined by the test logic. There are two options. First, the pin state may be determined by the data held in the boundary scan register, shifted onto the latched parallel outputs of the register during each pass through the scan sequence for the register. Second, every system output pin may be forced to an inactive drive state (e.g., high-impedance).

**CLAMP.** This instruction allows fixed guarding values to be placed on signals that control the operation of logic not involved in the test, but does not require that the Boundary-Scan register be part of the serial scan path as in the EXTEST instruction. The contents of the Boundary-Scan register will solely define the state of the system outputs upon the falling edge of TCK in the UPDATE-IR state for this instruction. The BYPASS register is connected between TDI and TDO in the SHIFT-DR state. This instruction is optional under the guidelines of IEEE Standard 1149.1 and therefore the binary code/s may be device specific.

**IDCODE.** (SCAN ABT and PSC110F only.) This instruction allows a blind interrogation of an identification code that is unique to this device type. During this instruction the IDCODE Register is connected between TDI and TDO in the SHIFT-DR state.

**USERCODE:** The purpose of this instruction is for user-programmable component, such as FPGA and EEPROMs. This instruction allows an external tester to determine the user programming of a programmable component.

**HIGHZ.** This instruction allows all of a components system outputs to be placed in an inactive drive state to permit its outputs to be safely back driven during testing of other integrated circuits on the printed circuit board. All outputs of the device will become inactive even if during their normal system function they are two-state outputs. The BYPASS register is connected between TDI and TDO in the SHIFT-DR state. This instruction is optional under the guidelines of IEEE Standard 1149.1 and therefore the binary code/s may be device specific.

**BYPASS:** This instruction allows rapid movement of test data to and from other components on a board that are required to perform test operations by selecting the BYPASS register, a single-bit shift-register stage, between TDI and TDO in the SHIFT-DR state to provide a minimum-length serial scan path. This instruction is mandatory under the guidelines of IEEE Standard 1149.1.

### III. CONCLUSION

IEEE Std. 1149.1-2001 also defines pin constraints standard and Boundary Scan Description Language which is not discussed in this paper.

Implementing boundary scan can reduce test costs, improve product quality and actually simplify the time, effort and cost of producing a product. For instance, developing traditional test vectors to test a complex IC can take months. Developing an I/O connectivity test with boundary-scan tools can take only minutes.

As silicon continues to shrink, packaging and board construction scale as well. At the same time, end-product quality is not an easy "given." From growing warranty costs, scrap-piles and unhappy customers, to plentiful industry studies, there is ample evidence that more defects ship than manufacturers think. To address these multiple challenges, effective test must be integrated throughout the product life cycle with minimum disruption and maximum results.

The "cheaper-smaller-faster-more features" syndrome affects everyone. Currently, almost all processors, FPGAs, CPLDs and ASICs have boundary scan designed into them. Recent memory devices from Cypress and Micron include boundary scan. The biggest missing players are the ASSP (application specific standard product) products in the computer business that were once considered not to be boundary-scan candidates. Yet an IC programmer at Apple recently shared that boundary scan is now essential to testing iMACs and notebooks. The momentum is definitely towards putting boundary scan in digital devices as the default.

### REFERENCES

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**Reviewer:** Gefu Xu

**Comments:** This paper gives a clear picture of Boundary Scan Standard within only four pages. A reader like me, who knows nothing about boundary scan, can grasp the basic concept of boundary scan standard with this paper. I think a more detailed description in the second part is better. In order to keep the length of the paper within 4 pages, the summary of boundary scan description language can be deleted.