

ELEC 7250 - VLSI TESTING

Term Paper

On

Analog Test Bus Standard

Muthubalaji Ramkumar

Analog Test Bus Standard

Muthubalaji Ramkumar
Dept. of Electrical and Computer Engineering
Auburn University

Abstract

This paper is a brief overview of the Analog Test Bus with the IEEE 1149.4 standard which illustrates the testability structure for mixed-signal circuits. The architecture provides the means of control of and access to both digital and analog test data. The key is the elimination of the need for physical probing of data at the pins, which is achieved by building an electronic test-access mechanism (the boundary-scan path) into the integrated circuits. The technical description of the analog test bus and an example of the usage of the test bus to perform impedance measurement is presented to show the test bus as an essential tool in system manufacturing test.

1. Introduction

Integrated Circuits with analog, digital logic and memory on the same substrate, forming a complete electronic system called Systems-On-Chip (SOC), replacing the Printed Circuit Boards (PCB), have become a visible R&D trend in recent years. To facilitate testing of SOC, IEEE developed an effective mixed-signal test technology - the P1149.4 standard. The P1149.4 standard is an extension of the 1149.1 standard – a structured framework for system-level test development which covers only digital systems and barely mentions analog and mixed-signal systems. The Analog Test Bus with the P1149.4 standard has become an important tool in the characterization and debug of analog and mixed-signal designs. The purpose of this type of test bus is to provide a simple, robust method to access key internal analog nodes of the system to verify specific signal characteristics and ascertain some component values. But for these access points, measurements taken through other circuitry can be expensive and time consuming.

2. Scope of the Analog Test Bus Standard

The P1149.4 standard provides the capability to find analog circuit faults like interconnect shorts and opens, misloaded discrete analog components. Moreover, some parametric test operations are also possible, such as measuring the impedance of discrete components and checking the DC threshold levels at various points. The Analog test bus standard effectively maximizes visibility into any device performance issues and provides valuable debug data for designers.

3. The basic P1149.4 architecture

As mentioned earlier, the 1149.4 (Dot 4) standard is an extension of the 1149.1 (Dot 1) standard with the following inclusions:

- An Analog Test Access Port (ATAP) with two pins (AT1 and AT2). AT1 used to drive analog values into the core circuitry or analog pins, and AT2 used to monitor the responses to analog stimulae (AT1 and AT2 can reverse their roles).
- An internal analog test bus consisting of at least two lines (AB1 and AB2), which is used to route analog stimulae into and out of the chip (core circuitry or analog pins).
- A test bus interface circuit (TBIC), inserted between the ATAP pins and the internal analog test bus, which defines the type of connections and signals present in these analog lines.
- Analog boundary modules (ABM), inserted between analog pins and core circuitry. The boundary modules are the P1149.4-equivalent of the Boundary scan cells in 1149.1, which in P1149.4 are called ABMs and DBMs (digital boundary modules, in this case associated with digital I/O pins).

The basic P1149.4 architecture is illustrated in figure 1, where the four additional structures referred above are shown.

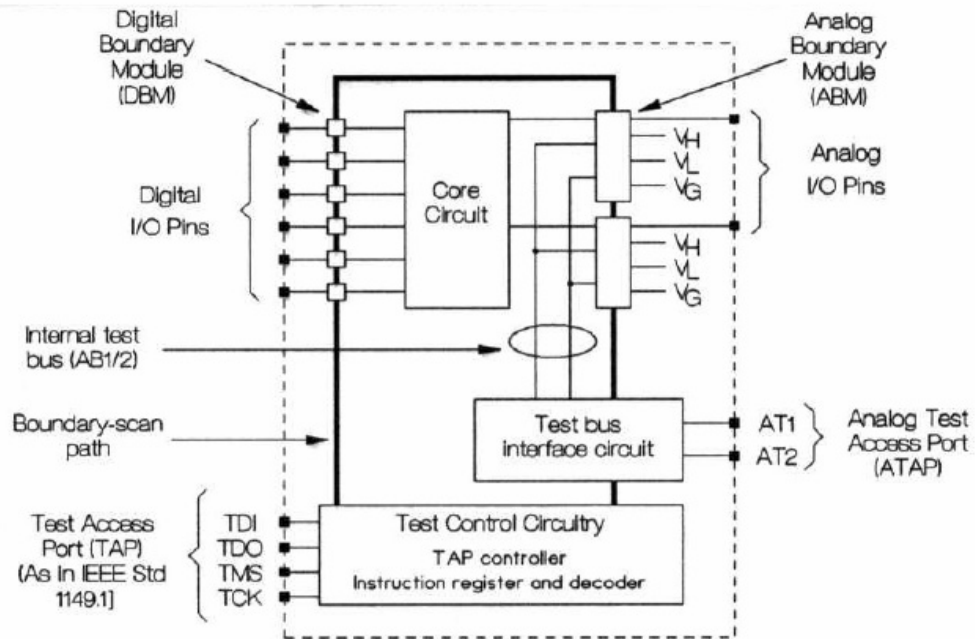


Figure1. The basic P1149.4 architecture

The operation of the P1149.4 infrastructure may be summarized as follows:

- An analog input is externally applied to AT1 and the analog output is monitored at AT2
- AT1 and AT2 are connected to the two-wire internal test bus, AB1 and AB2 respectively
- From AB1 the signal can be routed to the core or to a function output pin
- Responses are routed to AB2 from the core or from a function input pin

4. The Test Bus Interface Circuit (TBIC)

The TBIC controls the connections between the ATAP and the internal analog test lines. The switching architecture of the TBIC may be represented as shown in figure 2.

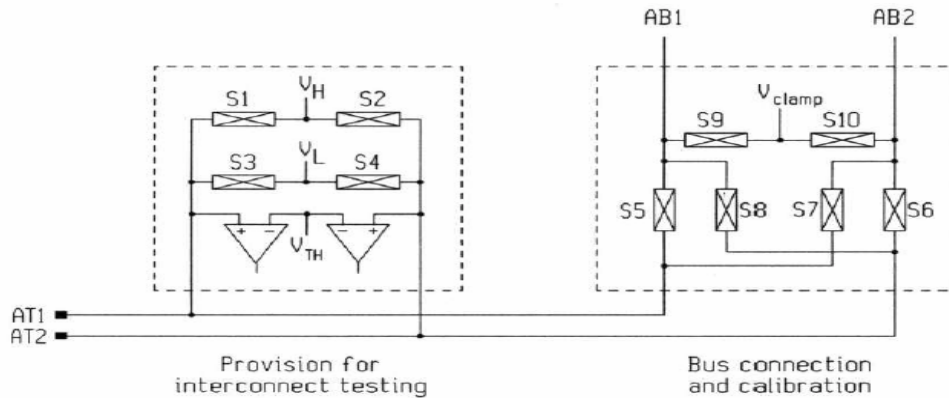


Figure2. Switching architecture of the TBIC

The switching architecture of the TBIC allows:

- AT1 Or AT2 to be connected to V_H or V_L
- AT1 or AT2 to be connected to AB1 or AB2
- AT1 or AT2 to be connected to the internal voltage source V_{CLAMP}
- A 1-bit representation of the voltage at AT1 or AT2 as compared to V_{TH}

5. The Analog Boundary Modules (ABM)

The ABMs are the heart of the P1149.4 architecture. Test signal application and response capturing through the ABMs takes place by combining serial access to the boundary-scan register and analog stimulae access to the ATAP. The switching architecture of each ABM is represented in figure 3. The condition (on/off) of the switches is defined by a control structure.

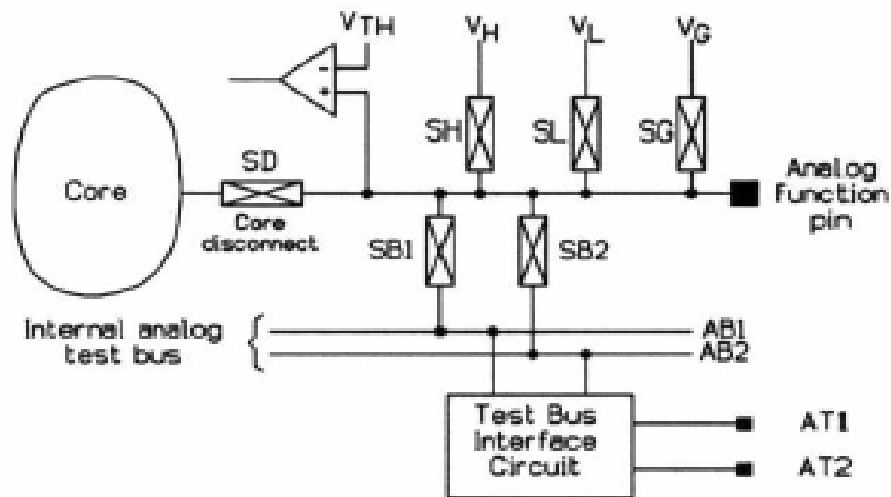


Figure 3. Switching architecture of the ABMs

The switching architecture shown provides the following functions:

- To disconnect the core from the function pin
- To drive the pin from AB1 (controllability)
- To drive AB2 from the pin (observability)
- To monitor a 1-bit representation of the voltage on the pin as compared to V_{TH}
- To connect V_H or V_L to the pin (for interconnect test)
- To connect a reference quality voltage V_G to the pin (for parametric measurements)

6. Instruction Set

Besides the mandatory 1149.1 instructions, P1149.4 defines MEASURE and PROBE instructions as the central feature of this standard.

- The MEASURE instruction is used to test interconnect of a simple wire, interconnect with passive components, differential and extended interconnects
- The PROBE instruction allows the analog pins on an IC to be driven by AB1 and monitored on AB2. This mode of operation safeguards against back driving mechanisms and other harmful effects.

7. Impedance Measurement Example

The full power of the P1149.4 standard is best appreciated by an example of impedance measurement between a pin and ground. The set up is shown in figure 4.

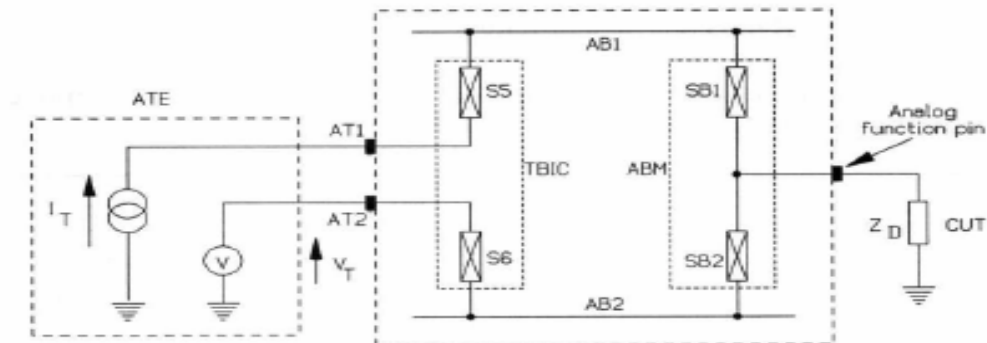


Figure 4. Test setup for measuring impedance between pin and ground

The measurement procedure may be summarized as follows:

- A known current I_T is applied through AT1, by way of switches S5 and SB1, to the unknown impedance Z_D
- The resulting voltage V_T is measured at AT2 connected to Z_D through S6 and SB2
- The Value of Z_D is computed as $Z_D = V_T / I_T$

8. Conclusion

The salient features of the Analog test bus standard are improved pin accessibility, measurements of continuous variables such as resistance, capacitance and delay, and direct control and observation of voltages and currents in continuous time. The primary benefit is increased diagnosability, which can reduce design verification time and cost. The provision of general purpose analog and digital facilities at every node of interest, via the standard access bus, provides a framework and gateway for Built-in Self Test (BIST). Moreover, the standard has changed the landscape of analog design as well, freeing the designer to concentrate on interesting new circuits rather than endlessly rehashing old ones.

9. References

1. "Analog and Mixed-Signal Boundary-Scan – A guide to the IEEE 1149.4 test standard" — edited by Adam Osseiran.
2. "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits" — Michael L. Bushnell and Vishwani D. Agrawal.
3. "Testing in a mixed-signal world" — Vishwani D. Agrawal, ASIC Conference and Exhibit, 1996. Proceedings, Ninth Annual IEEE International, 23-27 Sept. 1996.
4. "P1149.4 Mixed-Signal Test Bus" — Adam Cron, Design & Test of Computers, IEEE, Volume: 13, Issue: 3, Fall 1996.

Review – Arun Balaji Kannan