

# Fault Collapsing

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## Abstract

Fault collapsing is a very important approach to reduce overlapped stuck at faults and then generate effective faults in a digital circuit. It can greatly lessen the burden of the test generation and test work. In this paper, two types of fault collapsing methods are discussed. One is the equivalence fault collapsing which uses the conception of fault equivalence to delete most of the equivalent faults. The other is dominance fault collapsing which uses the conception of fault dominance to further eliminate the dominating faults from the equivalence collapsed faults. The dominance collapsed faults is normally less than half of the original total faults. Some complicated conditions, circuits with fanouts are discussed in detail. All stuck at faults on a fanout stem can not be deleted in equivalence fault collapsing, and part of faults on a fanout branch can not be deleted in dominance fault collapsing. The test results of benchmark circuit 74181 show that the collapsed ratio are 58.7% and 39.6% for equivalence fault collapsing and dominance fault collapsing respectively. Although the lower collapsed ratio of dominant fault collapsing, it is not as popular as equivalence fault collapsing because the dominance relationship maybe be invalid in some circumstances. Therefore, the equivalence fault collapsing is often recommended.

## 1. Introduction

A digital circuit can be modeled as an interconnection of Boolean gates. Each interconnecting line can have two types of faults: stuck-at-1 and stuck-at-0. Therefore, an n-line circuit can have at most  $2n$  single stuck-at faults. But, this number can be further reduced by the fault collapsing techniques [1]. In the following text, we will discuss two types of fault collapsing techniques—equivalence fault collapsing and dominance fault collapsing, which can greatly reduced the number of stuck at faults in a circuit.

## 2. Fault Equivalence

Two faults of a Boolean circuit are called equivalent if they have exactly the same set of tests and transform the circuit such that the two faulty circuits have identical output functions.[1] Let's take the example of a two input AND gate in Fig. 1. The stuck-at-0 faults on any input line of this AND gate can lead to a zero output which is the same faulty result of the stuck-at-zero fault on this gate's output line, and these three faults have the same test vector (1,1), therefore, for a two input AND gate, the two input stuck-at-0 and one output stuck-at-0 faults are equivalent. Because of the indistinguishability of equivalent faults, only one of them needs to be tested.

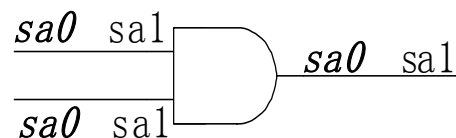


Fig.1 Fault Equivalence in AND gate

The equivalent faults in other Boolean gates can also be derived in the same way. But what is the relation between faults on a fanout stem and on fanout branches? In Fig 2, take the example of the three stuck-at-0 faults, although they have the same test vector (1), but the faulty circuit are not surely have the same faulty functions. Therefore, no faults on fanout stem and fanout branch are equivalent.

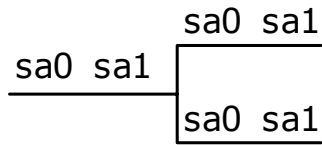


Fig.2 Fanout Stuck At Faults

### 3. Equivalence Fault Collapsing

Using the conception of fault equivalence, we can collapse or delete most of equivalent faults. This procedure is called equivalence fault collapsing, which partitions a circuit into disjointed equivalence sets, chooses one fault from each equivalent sets, and forms an equivalent collapsed fault set. For example, in Fig.3, because of the equivalence of the three stuck-at-0 faults in a AND gate, two of them can be collapsed.

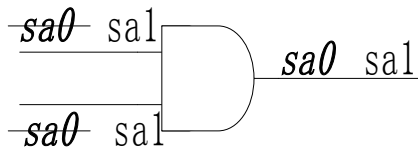


Fig. 3 Equivalence fault collapsing

When performing equivalence fault collapsing, we always delete the faults on the input lines and keep the fault on the output line. Therefore, two stuck-at

faults on a fanout stem, which can only be one gate's output line but not be one gate's input line, can not be deleted. (See Fig.4) So, to find which stuck at faults are on a fanout stem line is important to equivalence fault collapsing.

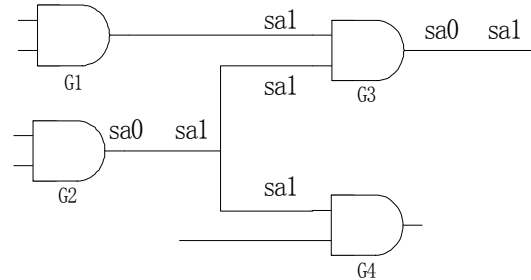


Fig 4 Fanout in Equivalence Fault Collapsing

### 4. Fault Dominance

If all tests of fault F1 detect another fault F2, then F2 is said to dominate F1 [1], and fault F2 can be deleted. Take the example of an AND gate, in Fig.5, to test F1, we should apply the test (0, 1). To test F2, we could apply any one of the following tests: (0,0), (0,1), (1,0), which include the test (0,1) used to test fault F1, therefore, we can determine that F2 dominate F1 and F2 as a dominating fault can be deleted. Normally, the gate output stuck-at fault dominates the gate input stuck-at faults.

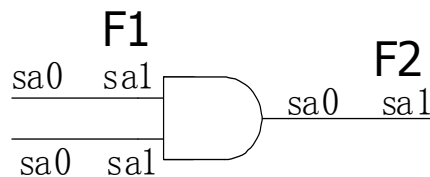


Fig.5 Fault Dominance

### 5. Dominance fault collapsing

Using the conception of fault dominance, we can collapse or delete all

the dominating faults. Actually, when performing dominance fault collapsing, we use the conception of equivalent faults simultaneously and further eliminate the dominating faults from the equivalence collapsed faults, that is the reason why dominance collapsed faults is normally less than half of the original  $2n$  faults.

For instance, in Fig 6, because the dominance of output SA1 to any input SA1, it can be deleted. At the mean time, three SA0 faults are equivalent, and two of them can be deleted. Because the dominance fault collapsing direction is from output to input, we normally firstly delete the output SA1 fault and then delete any one of two SA1 faults. From Fig. 6, it is also not difficult to find that faults on a gate's output line is deleted with priority during dominance fault collapsing.

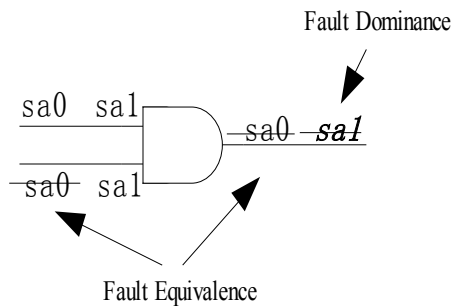


Fig 6. Dominance fault collapsing

Therefore, some stuck-at faults on a fanout branch, which can only be one gate's input line but not be one gate's output line, can not be deleted. (See Fig.7) Like equivalence fault collapsing, to find which stuck at faults are on a fanout branch line is important to dominance fault collapsing. For a fanout-free circuit, all dominance collapsed faults are located on the primary input lines. [1]

But if for a AND gate, one input line is on a fanout branch line and the other is

not, which input equivalent fault we should choose to delete?

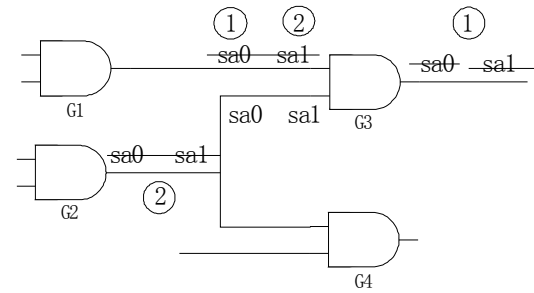


Fig.7(a) Select Fanout Branch in Dominance fault collapsing

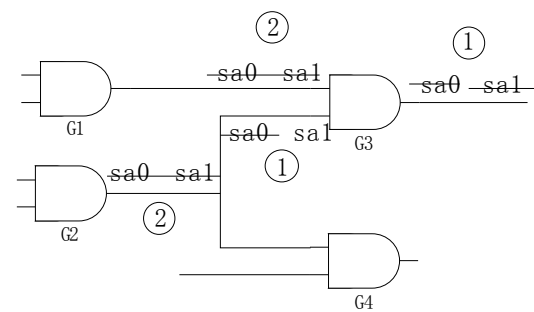


Fig. 7(b) Select non-Fanout Branch in Dominance fault collapsing

Take gate G3 in Fig 7 as an example. In Fig 7(a), if in step 1 we choose delete SA0 on the non-fanout branch input line, at last G3 will have two faults left, because faults on fanout branch line can never be deleted in the following fault collapsing step (step 2). If we choose delete SA0 on the fanout branch input line (Fig. 7(b)), G3 will have only one fault left, because the faults on the other non-fanout branch input line can be eventually deleted in the following collapsing step( step 2). As a result, in dominance fault collapsing, we should delete faults on a fanout branch line with priority.

## 6. Comparison of Two Types of Fault Collapsing

Because Dominance fault collapsing is to further reduce the dominating faults from the equivalence collapsed faults, the number of dominance collapsed faults is normally less than half of the original  $2n$  faults. Table 1 shows the test results for benchmark circuits, c17 and 74181.

Circuit Name	Total faults	Equivalence collapsed Faults	Dominance collapsed Faults
C17	34	22 (64.7%)	16(47.0%)
74181	404	237(58.7%)	160(39.6%)

Table 1. Fault collapsing comparison

Dominance fault collapsing can get a much lower collapse ratio compared with equivalence fault collapsing. This is obvious an advantage of dominance fault collapsing. But it has its own shortcomings.[1] The dominance relationships in a combinational circuit maybe invalid when that circuit is embedded in a sequential circuit because a fault can dominate several faults. A dominated fault may also become redundant due to circuit structure. Even though some dominating faults can be detected, no test can be generated for them because they are not in the dominant fault lists.

These above two disadvantages limit the use of fault collapsing and equivalence fault collapsing is often recommend. [1]

## 7. Conclusion

Fault collapsing is an essential part of any test system. The underlying algorithms are considered to be matured. [2] However, there still is plenty of research work in this area. A.V.S.S. Prasad *et al.* in their paper [2] presented

a new algorithm which can perform fault collapsing in a hierarchy circuit.

With the fault collapsing approach, the number of single stuck at faults in a digital circuit can be significantly decreased which is a great help to lessen the task of test. Between the two types of fault collapsing, although dominance fault collapsing has a lower collapsed ratio, equivalence fault collapsing is more popular.

## Reference

- [1] Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits, Bushnell & Agrawal, Kluwer Academic Publishers, 2000
- [2] A New Algorithm for Global Fault Collapsing into Equivalence and Dominance Sets, A.V.S.S.Prasad, Vishwani D. Arawal, Madhusudan V. Atre, 2002 ITC Internation Test Conference