STAFAN: Statistical Fault Analysis

Submitted by Malinky Ghosh

Reveiwed by Jyothi Chimakurthy

Abstract— **ABSTRACT- Statistical Fault analysis is used as an alternative to the fault simulation in digital circuits. The analysis requires only the fault free simulation of the circuit. It utilizes the calculation of controllabilities and observabilities of the circuit nodes which are further computed as the probabilities estimated from the signal statistics of the fault free simulation. The detection probability of a fault and fault coverage are computed further from the appropriate controllability and observability. These parameters are seen to be agreeing favorably with the fault simulator results. Thus STAFAN has a much less computational overhead compared to the regular fault simulators.**

I. INTRODUCTION

The continuing development of the manufacturing technology has lead to an increase in the density of gates possible on integrated circuits, with the result that access to their internal nodes is more difficult. Therefore there is a growing concern about the ease of testability of these integrated circuits. The use of fault simulators is very common thus to test the faults in these circuits. But the complexity of fault simulators are know to grow as square of the number of gates in the circuit. In this paper we describe about the statistical Fault analysis which requires only the fault free simulation that is considered much less complex as compared to faulty circuit simulation. The detection of any particular fault is computed using the probability of controlling the value on a line and propagating the value to the primary output. Thus STAFAN uses the concepts of controllability and observability. This method is useful for combinational as well as sequential circuits. It adds only a small overhead on the fault free circuit simulation. The statistical nature of it also gives higher accuracy to it. Thus it can be proposed to be better than other alternatives to fault simulation like critical path tracing as they can be used only for combinational circuits.

II. THEORY

The circuit consists of Boolean, single output, multiple input gates. The paths connecting the gates are called lines. The bit value for every line is calculated for the fault free system. The primary inputs of the circuit are fed with input vectors. We can have more than one input vectors. Here we consider N input vectors at a time.

Controllability and Observability are defined as:

Cl (*l*) or one-controllability of line *l* is the probability of line *l* having a value 1 on a randomly selected vector.

C0 (*l*) or zero-controllability of line *l* is the probability of line *l* having a value 0 on a randomly selected vector.

Bl (*l*) or one-observability of line *l* is the probability of observing the line *l* at a primary output when the value of line *l* is 1. This is the conditional probability of sensitizing a path from line *l* to a primary output, given that the value of line *l* is 1. Similarly,

B0 (*l*) or zero-observability of line *l* is the path sensitization probability from line *l* to a primary output when the value of line e is zero.

The controllability value is thus the probability of setting the corresponding circuit node to a particular value and the observability value is the probability of propagating this value to one or more primary outputs. The zero or one controllability is given by the number of times the node takes a value one or zero respectively divided by the total number of input vectors. Thus for every gate in the circuit we have a one counter and a zero counter which counts the number of times the output line of the gate assumes the value one and zero. When the line assumes an unknown value none of the counters are updated. Similarly when a line takes a high impedance value the counter incremented last is incremented again. Every line in the circuit has a sensitization counter. This counter is incremented when the path from the corresponding line to the output is sensitized. Thus when the number of one counters and zero counters vary with the number of gates in the circuit the number of sensitization counters vary with the number of lines in the circuit. The one and zero counters are used to compute the corresponding controllability and the sensitization counter is used for the observability. The controllability are given by

$$\mathrm{C0}\ (l) = \frac{one\_count}{N}$$

$$\mathrm{C1}\ (l) = \frac{zero\_count}{N}$$

As incase of controllability, the sensitization probability for line *l* is given by

$$\mathrm{S}\ (l) = \frac{sensitization\_count}{N}$$

For the primary output observability is set to 1, that's the minimum value for observability. The circuit is then back traced until the observabilities of each node are obtained. The 0 and 1 observabilty is calculated as the probability that the corresponding logic value on that input will propagate to the gate output, multiplied by the corresponding observabilty of the gate's output node.

Consider the three input gates shown in Fig. 2. Lines j, k and l are the input lines and m is the output line. From the definition of controllability and observability we derive the following formulae.

For AND gate:

$$C1(m) = Probability\ \{j=1, k=1, l=1\}$$
$$= Probability\ \{j=1, k=1 \mid l=1\}.\ C1(l)$$

thus, $Probability\ \{j=1, k=1 \mid l=1\} = C1(m)/C1(l)$

Now froom the definition of observability, to observe the value of line l =1

$$B1(l) = B1(m).\ Probability\ \{j=1, k=1 \mid l=1\}$$
$$= B1(m).C1(m)/C1(l)$$

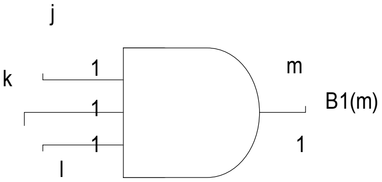

Figure 1: Showing observability of line m

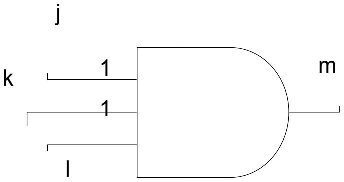

Figure 2: Showing sensitization of path from l to m

For sensitization probability of line l, the path from line l to output should be sensitized. For this all the other input to the gate should have non controlling values on them. Thus,

$$S(l) = Probability\ \{j=1, k=1\}$$
$$= Probability\ \{j=1, k=1, l=1\} + Probability\ \{j=1, k=1, l=0\}$$
$$= C1(m) + Probability\ \{j=1, k=1 \mid l=0\}.C0(l)$$

Therefore, $Probability\ \{j=1, k=1 \mid l=0\} = \dfrac{S(l) - C1(m)}{C0(l)}$

Now zero observability is defined as

$$B0(l)=B0(m).\ Probability\ \{j=1, k=1 \mid l=0\}$$
$$=B0(m).\ \frac{S(l) - C1(m)}{C0(l)}$$

For OR gate,

$$B1(l)=B1(m).\ \frac{S(l) - C0(m)}{C1(l)}$$
$$B0(l)=B0(m).C0(m)/C0(l)$$

For NAND Gate

$$B1(l)=B0(m).C0(m)/C1(l)$$
$$B0(l)=B1(m).\ \frac{S(l) - C1(m)}{C0(l)}$$

For NOR Gate

$$B1(l)=B1(m)\ \frac{S(l) - C1(m)}{C1(l)}$$
$$B0(l)=B1(m)\ \frac{C1(m)}{C0(l)}$$

For NOT gate

$$B1(l)=B0(m)$$
$$B0(l)=B1(l)$$

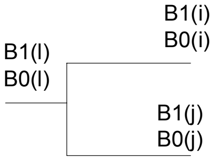

Figure 3: showing the fanout structure

Further, in digital circuits the occurrences of fanouts are common. The analysis of 0 observabilty is presented recognizing that the same is true for 1 observability too. For fanouts the the upper and the lower bounds of the observabilities are calculated. The value of line l can be observed on either fanout lines i or j. So, we take the maximum of the two observabilities as the lower bound for line l.

Therefore,

$$B0(l) >= max[B0(i), B0(j)]$$

If the output paths through i and j are completely different and independent we can take it to be the joint probability (assumed independent) of the observabilities to be the observability of line l. Thus,

$$B0(l)=B0(i)+B0(j)-B0(i).B0(j)$$

This gives the upper bound of the observability of line l. To account for the degree of reconvergence of the circuit under consideration we introduce a factor α , such that

$$B0(l) = (1-\alpha) \max_{1 \le k \le m} [B0(i_k)] + \alpha \left\{ \bigcup_{k=1}^{m} B0(i_k) \right\}$$

Here α = 0 indicates minimum observability of line l and α = 1 indicates maximum observability of line l.

III. CIRCUIT EXAMPLE

The circuit used for example consists of a single NOR gate with output fed back to the input. This simple example is chosen to demonstrate the STAFAN calculations without much complexity. Assuming that the signal on line 1 and 6 are independent, we are left with calculation of the observability of line 3 and 4. Since the circuit has feedback we use an iterative expansion of the circuit as shown. The iteration number is hereby referred to as the order of calculation, denoted by the subscript of B. Let the $B1_0(4) = 0$ is the zero order value of one observability of line 4 and also let the observability values of primary output line 7 and 8 be known.

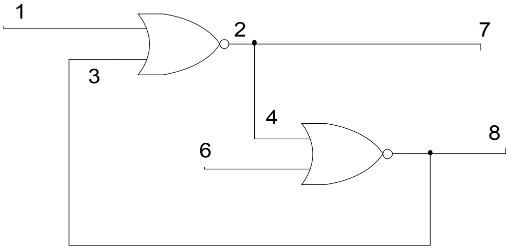

Figure 4: the example circuit with feed back on line 3

Then,

$$B1_0(2) = (1-\alpha)\max\{B1_0(4),B1(7)\}+\alpha[B1_0(4)+B1(7)-B1_0(4).B1(7)]$$

$$= B1(7)$$

$$B0_0(3) = B1_0(2).\ \frac{C1(2)}{C0(3)}$$

$$= B1(7).\ \frac{C1(2)}{C0(3)}$$

$$B0_0(5) = (1-\alpha)\max\{B0_0(3),B0(8)\}+\alpha[B0_0(3)+B0(8)-B0_0(3).B0(8)]$$

$$B1_1(4) = B0_0(5)\ \frac{S(4)-C1(5)}{C1(4)}$$

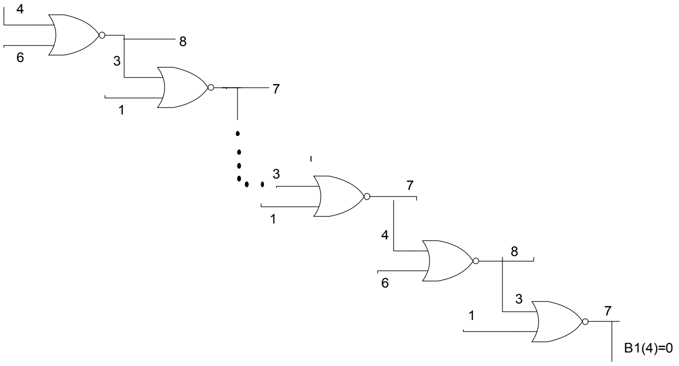

Figure 4: Iterative expansion of example circuit.

Once these are calculated the values for line 1 can be easily calculated using the above mentioned formulae. The one observabilities also can henceforth be thus calculated. After suppose n iterations if the n-th value of $B1_n(4) = x$ and also n is large enough such that

$$B1_{n+1}(4) = B1_n(4) = x$$

Then on writing expression $B1_{n+1}(4)$ in terms of x and on solving equation we get the value of x. Some circuits might have two or more primary inputs like the one mentioned here. If such a circuit is clocked we cannot assume the primary inputs to be independent. In that case it is required to calculate the loop sensitization probability of the circuit. This is accomplished by identifying all the primary input signals of the circuit.

These are simultaneously set to one. We set up a loop counter in such cases which counts the number of loops in the circuit. The loop sensitization probability in that case is given by

$$L = \frac{loop\_count}{N}$$

Now line 4 can be observed at line 7 directly or 8 after an inversion or throught the previous (n-1) vectors. The hatched OR gate leads to the next higher iteration say (n+1).

Therefore if this path is sensitized it goes to the next iteration observability. Now for this hatched gate, which indicates the presence of a loop the probability of sensitization is L. therefore here,

$$B1_{(n+1)}(4) = L.\ B1_{(n+1)}(4^*) = x$$

Where 4* denotes the obsevability after n+1 iterations and is produced due to fanout of B1 (7), B1 (8) and x. Now here x = L. (K + x - Kx) denoting fanout between K and x where again K is given by

$$K= (1-\alpha)\max\{B1(7),B0(8)\}+\alpha[B1(7)+B0(8)-B1(7).B0(8)]$$

Thus

$$x = \frac{LK}{LK+(1-L)}$$

IV. FAULT DETECTION PROBABILITY

Once the fault free circuit controllability and observability values are calculated we go ahead with the fault detection probability which on further computation gives us the required fault coverage values. We assume line l to have “stuck at one” fault on it. The fault is said to be detected when its effect is propagated to the output. For this the fault is sensitized by placing a 0 on the line. Thereafter, observing it at the primary output. The probability is thus given by

D1 (l) = Probability {Line l set to 0 and observing l}
= Probability {l is set to 0}. Probabilty{l observed|l = 0}
= C0 (l) . B0 (l)

Taking the detection probability for a vector is x. Thus the probability of the fault not being detected by this vector is 1-x . If N vectors are used, then fault not being detected by any of the vectors is given by $(1-x)^N$. Therefore detection probability of the fault by N vectors is given by

$$X(N) = 1-(1-x)^N$$

Since all the probabilities thus calculated are statistical estimates we can consider them to be random values such that $N \rightarrow \infty$. Assuming that the probability of certain fault detection is given by $p(x)$ and also that x_0 be the mean value of this random variable. We also assume that the value x varies in a range 2Δ such that the domain is $[x_0-\Delta, x_0+\Delta]$. Therefore the actuall probability of fault detection can be obtained by computing the expected value of the random variable $X(N)$.

$$E(1-(1-x)^N) = 1- E(1-x)^N = \frac{1}{2\Delta}\int_{x_0-\Delta}^{x_0+\Delta}(1-x)^N\,dx$$

Simplification gives us

$$= 1 - (1-x_0)^N\,[1 + \frac{N(N-1)}{3!}(1-x_0)^{-2}\Delta^2 + \ldots\ldots.]$$

$$W(x_0) = [1 + \frac{N(N-1)}{3!}(1-x_0)^{-2}\Delta^2 + \ldots\ldots.]$$

Therefore we can write as

$$X(N) = 1 - (1-x_0)^N / W(x_0)$$

Standard deviation given when detection probability is given by Bernoulli's trials is denoted by $b=\sqrt{\frac{x_0(1-x_0)}{N}}$

Thus using a constant of proportionality we get $\Delta= \beta\sqrt{\frac{x_0(1-x_0)}{N}}$

Thus

$$W(x_0) = [1 + \frac{(N-1)}{6}\beta^2\frac{x_0}{1-x_0} + \ldots\ldots.]$$

V. FAULT COVERAGE

Consider total V test vectors in all to test a circuit with K faults. These can be divided into k subsets such that $V/k = N$. The total fault coverage of the circuit can be obtained by

$$F(jN) = \frac{1}{K}\sum_{i=1}^{K} f_i(jN)$$

Where $f(jN)$ is the cumulative detection probability given by

$$f(jN) = 1 - \prod \frac{(1-x_{im})^N}{W(x_{im})}$$

VI. STAFAN OVERHEAD

As shown by the table we come to know the number of calculations required in STAFAN. G is the total number of gates in the circuit. The zero and one counter as mentioned above are required for every gate and thus total number of these counters required are G. These counters perform examination of the line value and thereafter update the line value. Thus the total operations are 2G. Assuming the average number of input lines per gate to be η; then total lines in the circuit, other than the primary outputs, are ηG. All these lines are required to have sensitization counter. Thus total numbers of these counters are given by ηG. In order to update this counter for a gate-input line, all other inputs of this gate must be examined. Thus total operations are $\eta^2 G$. The average number of loops in a circuit are less than G. Assuming the number of gates associated in a loop are η_l then the number of operation associated with this counter would be less than $(\eta_l + 1)G$. The total overhead is thus given by

$$\text{Overhead } \alpha\ G(4 + \eta^2 + a\eta_l + a)$$

Here a is a proportionality constant < 1 to take care of the operations associated with the loop.

On experimental implementation the value of α was found to be 1. This corresponds to the case that the fanout branches are independent. Similarly experimental results gave the value for $\beta^2/6$ to be 5. This produced good match with the fault simulation result.

VII. CONCLUSION

STAFAN is definitely an alternative to fault simulators. It's of great help for fault simulation of large circuits and produces very good results for the fault coverage. But two parameters α and β are determined empirically. β is determined from the fault simulation results, α depends on the circuit structure.

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