Low voltage operation of a 16 bit counter in 32 nm CMOS technology

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Abstract- In this report you will see a project based on 32 nm CMOS technology working both under and above its threshold voltages by manually adjust it Vdd voltage. There are many situations when a low voltage operation of a counter would be beneficial. The aim of this project is for saving power consumption. Let the 16 it counter working under very low voltage until it cannot functional well. And find the lowest working voltage and the voltage for best performance.

I. Introduction

POWER dissipation minimization is one of the prime concerns in recent VLSI design. As chip size is shrinking and many other micro-electronics reliabilities are developing gradually, low power design of any system has become priority. Computer system consists of sequential circuits mostly and that is why efficient low power design of various sequential circuits is very important. Low power circuit design is one of the vital concerns in VLSI design now-a-days. Power dissipation was not a very important issue at the beginning of VLSI design. But as the system feature size is shrinking gradually and clock frequency is developing rapidly, power issue has become one of the prime concerns for system designers. Several researches are being conducted to ensure low power design of several systems.

There are different kinds of power dissipations occur in CMOS devices. Basically they are of two kinds: Static dissipation and dynamic dissipation.

Sub-threshold current in inactive transistor, oxide gate tunneling current, reversed biased diode leakage, contention current etc. are known as static power dissipation. Load capacitance discharging current and switching mode short circuit current cause dynamic power dissipation in CMOS devices. Among all these dissipations, short circuit current dissipation plays a major role in power dissipation in sequential circuits. As sequential circuits are operated by clock pulses, there are short circuit dissipations in each clock transition in the system. Short circuit dissipation will be elaborately discussed in the following point. In short, the goal of this project is obviously, that according to the formula:

$$P_{total} = P_{dyn} + P_{stat} = P_{tran} + P_{sc} + P_{stat}$$

here: $P_{trans} = E_{trans}\, \alpha\, f_{ck} = \alpha\, f_{ck}\, CV^2/2$

I can test the power consumption by gradually decrease the vdd voltage and meanwhile keep the 16 bit counter functional well.

II. Counters

In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. The most common type is a sequential digital logic circuit with an input line called the "clock" and multiple output lines. The values on the output lines represent a number in the binary or BCD number system. Each pulse applied to the clock input increments or decrements the number in the counter.

A counter circuit is usually constructed of a number of flip-flops connected in cascade. Counters are a very widely-used component in digital circuits, and are manufactured as separate integrated circuits and also incorporated as parts of larger integrated circuits.

And there are, in general, 4 kinds of counter can be used in my project.

1,Asynchronous (ripple) counter – changing state bits are used as clocks to subsequent state flip-flops
2,Synchronous counter – all state bits change under control of a single clock
3,Decade counter – counts through ten states per stage
4,Up/down counter – counts both up and down, under command of a control input.

Finally, I chose the synchronous counter with JK flip-flop see in Fig 1 for the following reason:

In synchronous counters, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel).

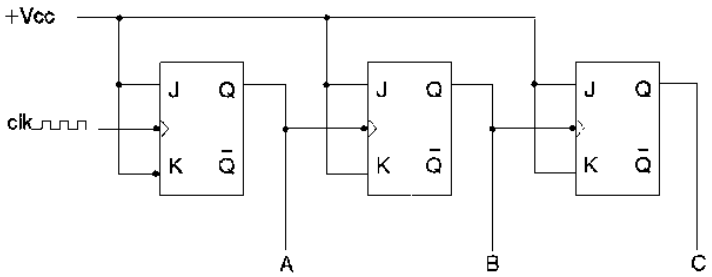

Fig 1 one kind of 3bit synchronous counters with JK flip-flop

On the other hand, by using synchronous counters we can get rid of the ripple effect problem by clocking every flip-flop simultaneously. All of the flip-flops make their transitions at the same time, and the information travels from the output to

the input before the next rising edge of the clock. In a synchronous counter the indeterminate period of all of the flip-flops is the same, but as with the asynchronous counter, the delay of each flip-flop still increases as the number of bits grows. So, by using the synchronous counter we can greatly decreased delay of circuit than using other counters.

III. Circuit of 16 bit counter

In my design, first of all, I'm immediately think about the JK flip-flop with its differential frequency character deal with the clock frequency. I'm trying to extend the 3bit (See in Fig 2)binary counter into 16 bit binary counter with a 4 four bit counter. (See in Fig 3)

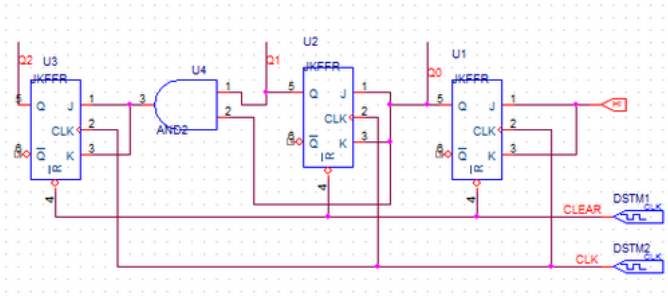

Fig 2 3bit counter

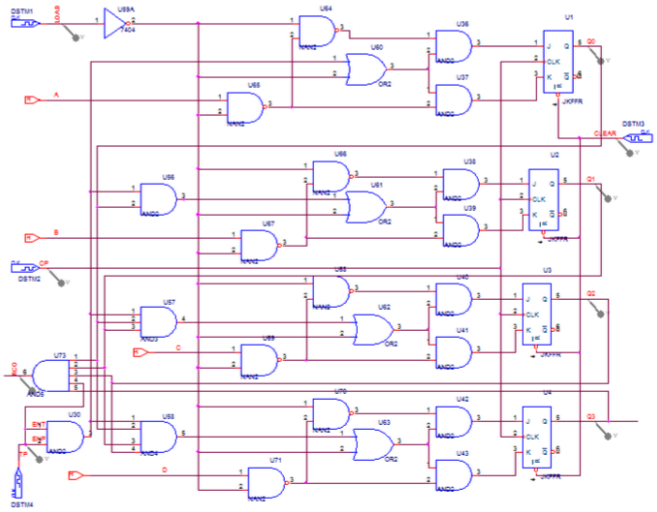

Fig 3 A, Four bit counter

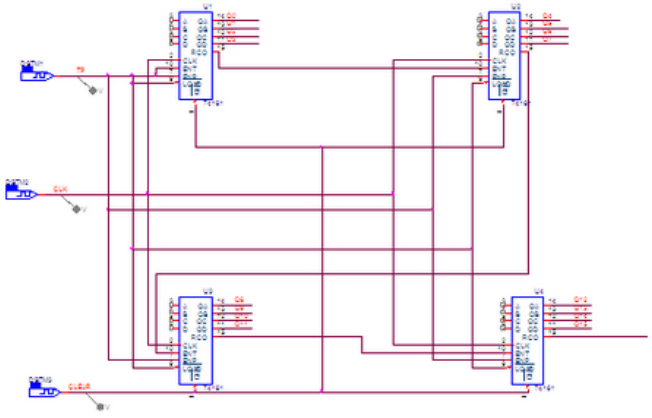

Fig 3 B, 16 bit counter

IV. Simulation

The design in my 16 bit counters in under 32 nm process technology. The PMOS and NMOS threshold voltages for these technologies are 0.49396V and -0.60155v respectively. With the VHDL code of binary counter, I use some of simulation software for the counter design. I use Design Architect-IC for Schematic Capture and I use Leonardo Spectrum and finally I use SPICE for circuit simulation and verification. And, here is the out wave of my 16 bit counter.(see in fig 4)

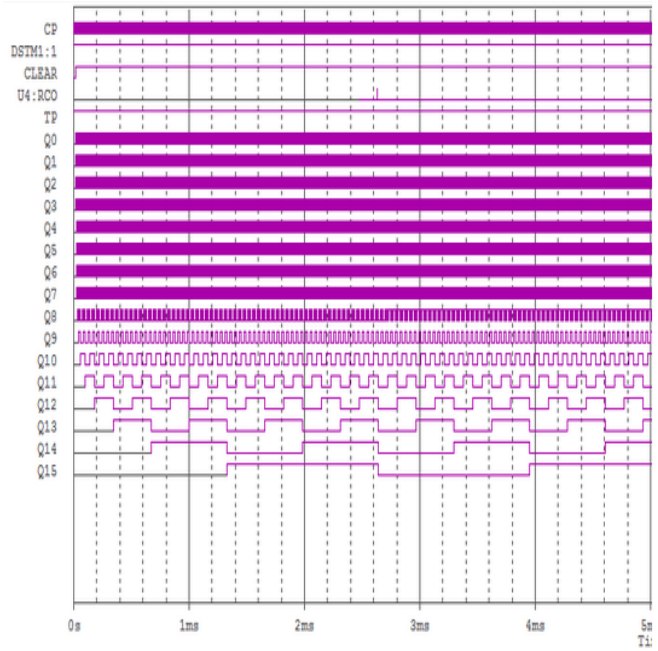

Fig 4 wave of the simuation

In order to make sure that this 16 bit counter is working with the best performance, I also measure the data of the critical path delay of the circuit.

V. Results

In my simulation, I measured total power consumption, and gate delay as well. Unfortunately, on the day of my presentation Dr.Agrawal point out and thanks a lot that I should not only decrease the voltage of in my simulation but also to proportionally change the clock frequency that make my simulation reasonable because I did not use the best or the best clock frequency to test my power consumption for different voltage. What have I learn from his kindness suggestion is I should, for example, is start with voltage A and also change the clock frequency until I find a clock frequency that matching the voltage A, a frequency B and doing the same procedure in the following steps. Here is the result of power dissipation as a function of voltage. (See in Fig 5) you can see here, the power decreased proportionally with the V

until the transistors can no longer function according the formula of the power consumption in our course slide

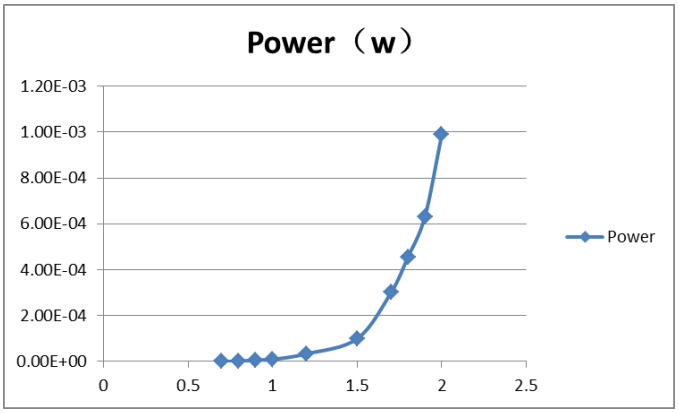

Fig 5 power dissipation with decease of voltages

According to the figure 5, it is obviously 1, power dissipation decreased as the decreasing of the voltages. 2, once I decrease the voltage under 0.8 V make this 16 bit counter no more functional. Actually, it should be keep working nearly 0.6V as its threshold voltages, while I think it is because I I didn't use the best clock frequency to finish this simulation that make the voltage which still above the Vth but not work well. And the value of 0.7 and 0.8 is under the 1.1 which is the values of the sum of Vth of Pmos and Nmos transistor.

In order to make sure the correct working of my 16 bit counter I also recorded the delay of the circuit that I expected (see in Fig 6), when the counter working above the sum of Vth of two transistor which mean it is working in the saturation area and the delay is roughly around 10 ns. Along with the keeping decrease of voltage that the counter can not working in the saturation area and the decreasing of the speed of circuit, the delay is greatly increased.

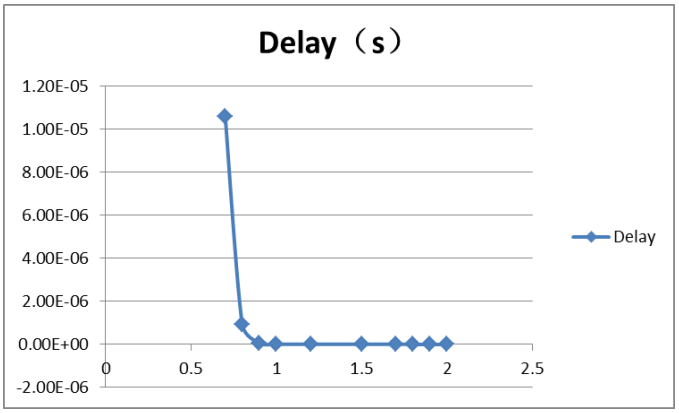

Fig 6 Delay

In order to find the optimal operating voltage I use the product of power and delay. And the best working point is at a minimum. This point is the voltage at which the circuit can operate that causes the least tradeoff between the power and delay. This operating voltage is approximately 1V and it is much higher than the 0.8v that only keep this counter operated well.

Here is the simulation data form of my 16 bit binary counter. (See in form 1)

16 bit binary counter	Power(w)	Delay(s)	power*delay
2	9.89 E-04	2.11 E-09	2.10E-12
1.9	6.32 E-04	2.92 E-09	1.75E-12
1.8	4.56 E-04	3.39 E-09	1.43E-12
1.7	3.01 E-04	4.69 E-09	1.20E-12
1.5	9.91 E-05	8.20 E-09	7.59E-13
1.2	3.32 E-05	9.90 E-09	3.35E-13
1	9.20 E-06	1.37 E-08	1.26E-13
0.9	6.51 E-06	6.90 E-08	4.13E-13
0.8	9.75 E-07	9.20 E-07	8.90E-13
0.7	5.32 E-08	1.06 E-05	5.63E-12

Form 1, power dissipation, delay and the product of power and delay

And I use excel to make a figure for this form to find the best operation voltages for my 16 bit counter.(See in figure 7). We can see that the best voltage that also means making a best balance between delay and the power dissipation with lowest point is around 1 V.

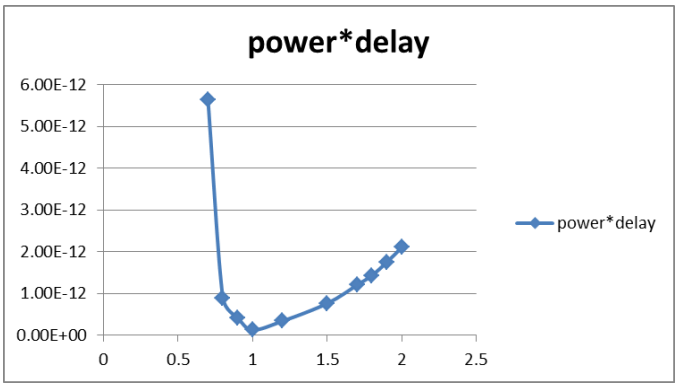

Fig 7 power dissipation*delay

VI. Discussion

Other than control or decrease the voltages for the low power saving in this project we should also consider other

factors like the process of the transistor and number of gate and which kind of gate should be used and can be used in our circuit that decrease the statistic power dissipation. We should also ask the circuit to sleep or shut down when we don't use the circuit. Actually, there are a number of other optimizing techniques could be performed to further reduce the power consumption.

VII. Conclusions

I do like this project that 16-bit counter in 32 nm and control its power dissipation. It is my first time to use and learn some basic simulation tools especially the SPICE and its basic function as well. By participate this course project, I'm able to understand what I just learned about the low power design in class. VLSI technology is ubiquities in our daily life and playing an important roles, so the power save technology should be well studied that make VLSI technology save more energy without sacrifice its speed.

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