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Power Reduction in a 32-bit Adder using Parallelism and Reduced Supply voltage

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***Abstract*— In this paper I have presented two adder designs, one is a 32 bit standard adder and the other is a combination of two 32 bit adders in parallel that consumes less power at lower supply voltages. The paper starts by giving a brief description of both the circuits that explains the functioning of the circuits and the components that I have used. This is followed by the comparison between the two circuits on the basis of Power dissipation at different supply voltage. The implementation of the two circuits is successfully shown in the report.**

*Index Terms*— 32 bit adder, HSpice, Low Power, Leonardo Spectrum, Design architecture (DAIC), Power analysis, supply voltage.

# INTRODUCTION

The need for energy and power reduction has grown exponentially over the years, but in recent times this reduction effort has emerged as one of the most urgent needs to overcome limiting factors in VLSI development. The main goal is to reduce power dissipation while maintaining adequate throughput rate. The need for this low power systems is increasing rapidly because its cost effective, increases reliability of the systems, produces less heat helping systems to run longer and faster.

 There are innumerable areas and approaches where power reduction can be attempted; the scope of this paper will be power reduction in a 32-bit adder through reducing supply voltage while using multiple adder logic cores in parallel. The basic goal is to reduce the supply voltage so that each logic core runs at 1/N the speed of a reference design with standard supply voltage; the N multiple cores provide the ability to maintain original throughput of a reference design with full

supply voltage. For this project N = 2 is used.

In this project a standard 32 bit adder and a Low power design were modeled using VHDL. The proper functioning of both the designs was verified in ModelSim. The designs were converted to verilog files using Leonardo Spectrum and Spice netlist was generated using DAIC. Power analysis was then performed to get significant and comparable results.

# Design Procedure

The number of transistors integrated on a single chip still dramatically increases with Moore’s Law. While processing the chip temperature goes really high which can destroy the chip. This high power makes the systems run faster and thereby making the design for chip cooling systems more complicated and expensive. Now a days, portable devices require their hardware to consume as low energy as possible that allows them to operate longer with a limited battery capacity. Therefore, low-power circuit design has become more important or even been a mandatory requirement.

Both the adder design used the technology file from the PTM (predictive technology model) website. The technology used in both the design is 45nm. In order to calculate the power dissipated by the design, random test vectors were applied to the two adders at the fastest clock possible.

All the components of the models were verified to work correctly before being combined in the top-level design. For the clock generator, an external clock with a period of 10ns was used; the generation of twin inverted clocks with period of 20ns is seen to be verified.

# Description of 32-bit adder

 Figure 1: Standard 32-bit adder

Fig. 1 shows the standard 32-bit adder. It has 64 bit input vector (2x32 bit), 33 bit output vector (32bit + 1) and there is one cycle delay for result. The frequency of the 32 bit adder is F and the time period is 1/F.

The 32 bit adder is implemented using combinational logic which is called into a top level model. The top level model clocks the whole circuit with the rising edge.

The codes for the 32-bit ripple carry adder were compiled in Modelsim to verify the outputs. The outputs obtained from the simulation of the circuit were as expected.

# Description of the Low power 32-bit adder

 Figure 2: Low Power 32-bit Adder

Figure 2 shows the Low power design of the 32-bit adder. It has the same inputs and outputs as the standard design. The 'CL' block takes in a frequency F and produces a divided down clock with frequency of F/2. Each adder uses a divided down frequency of F/2.

1. The low power model uses two 32-bit adders in parallel to lower the processing speed

2. The model was implemented on lower supply voltages which reduces gate delay and decreases frequency

3. The 'CL' block reduces the frequency to F/2 and feed that to the two adders in parallel. By reducing the frequency the critical delay of the circuit increases and the computation takes longer to complete and the circuit consumes more energy.

# Power Analysis

In order to do the comparison and get data, the above two circuits were first simulated in Modelsim. Then the Leonardo spectrum was used to get the synthesized verilog net list which was imported in Design architecture to get the SPICE net list. The SPICE net list was modified for 45nm technology and the HSPICE simulation was run for random vectors. The final output was checked using EZ waveform.

For the purpose of ease in calculation, each model would use an external clock of 100MHz for a 10ns period. Leonardo had calculated the critical delay for each model; I used this value and the 45 nm standard 1.5V used for frequency calculation with the formula F = k x (Vdd - Vt)/Vdd, where k is a frequency proportionality constant, and Vt is 0.34V for 45nm. This produced a k = 138.4MHz, which was then used to calculate frequencies at the following voltages:

|  |  |
| --- | --- |
| Vdd (V) | Frequency (MHz) |
| 1.4 | 141 |
| 1.2 | 99 |
| 0.9 | 86 |
| 0.7 | 71 |

Table 1: Vdd vs. Frequency

The 1.4V and 1.2V were chosen for the top model; 1.4V would provide a good amount of slack at 100MHz but provide a decent baseline to measure the reduced power. 1.2V would provide a supply voltage closer to 100MHz, which saves the power on slack and gives us a lower power. This value would be lower as compared to the power value at 1.4V. The power reduction of 1.2V would not be as much as in other cases with lower supply voltages.

The power reduction in case of 0.9V and 0.7V was much higher as compared to 1.2V. In both the cases the frequency lowers leading to the increase in the critical path delay. Other supply voltage values were also tested but the power generated from those values were orders of magnitude lower. Actually on lowering the supply voltage the frequency of the circuit decreases and it takes much longer for the output to be produced at the clock transition, and thus dynamic power is not dissipated. Therefore those voltage values were ignored power analysis.

|  |  |  |
| --- | --- | --- |
|  | Standard 32 bit adder | Low\_Power 32-bit adder |
| Vdd | 1.4V | 1.2V | 0.9V | 0.7V |
| Frequency(MHz) | 100 | 100 | 100 | 100 |
| Power | 649.38 | 407.62 | 167.44 | 154.81 |
| % Reduction(1.4V) | - | - | 74.21% | 76.16% |
| % Reduction(1.2V) | - | - | 59.01% | 69.02% |

Table 2: Table showing comparison of Power



 Figure 3: Change in power with voltage

A list of randomly generated vectors were created in a vector file. Those vectors were forced into each bit line of the input vector for simulation of power. The average power was measured using HSpice and verified using EZwave. The table above shows the comparison between the standard 32-bit adder and the low power 32-bit adder. From Figure 3 It can be seen clearly that as the voltage goes down the power dissipated decreases. The power reduction in case of low power 32-bit adder is much lower than standard 32 bit adder. There is close to 75% reduction in the power with respect to 1.4V supply voltage . Good power reduction is still seen with respect to 1.2V supply voltage.

Much of this power savings is due to the higher power produced by the standard model by producing the work much faster than it needs to. In the Low power design the frequency fed to the two parallel adders is F/2 therefore it takes longer for processing and we see low power dissipation. Once unnecessary speed above 100MHz is marginalized with the 0.9V supply, power savings of ~75% are seen; furthermore savings of nearly 60-65% are seen with 0.7V. It must be noted that even in the standard design as the supply voltage is reduced from 1.4V to 1.2V the power reduced by almost 37%. The reason for this is because lower supply voltage leads to lower frequency and thereby lower critical delay which in turn leads to lower power dissipation.

# Conclusion

In this project a standard 32-bit adder and reduced power 32-bit adder were successfully implemented. It was successfully shown through experimentation that implementing a parallel scheme for the functional components of a design and reducing the supply voltage to each parallel component can significantly reduce the power dissipation. The results are discussed in the above section. The functioning of the two circuits and there components were simulated in Modelsim simulator. Simulation results conﬁrmed the proper functioning of the two adder circuits.

Best results for comparison are against the 1.4V supply, where ~75% reduction was seen. This is a significant improvement over simply reducing the voltage and proves this scheme to be effective for power reduction.

# future work

A lot of work can still be done on this topic, such as instead of using 2 32-bit adders in parallel we can use 3,4,5 or more adders in parallel and we can measure power for this range parallel adder implementation. Another thing that can be done is to use a lower technology file like 32nm which would have more number of transistors. Moreover more efficient coding can also lead to a better design and computation

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