ELEC 5270-001/6270-001 Low-Power Design of Electronic Circuits   
Spring 2015

Homework 2 Problem

Assigned 3/11/15, due 3/18/15

**Problem:** Refer to slides 36-47 of Lecture 4 on Linear Programming.The one-bit full-adder on slide 39 is constructed with two-input NAND gates. Fanouts are shown in the diagram and note that the fanout of the carry output is 2. Two types of NAND gates are available, NAND(0) optimized for delay and NAND(1) optimized for power. Their delay and power, normalized with respect to a standard NAND gate with an inverter load, are as follows:

NAND(0), delay = fo, power = 3fo

NAND(1), delay = 2fo, power = 0.5fo

where fo is the fanout; fo is an integer ≥ 1. Use an ILP solver to design pwer optimized circuits for critical path delay Tc = 11, 15, 19 and 22. **Tabulate numbers of NAND(0) and NAND(1) used, power and delay for these designs. Sletch the circuit for Tc = 15.**

Note: MATLAB has an ILP solver that is available to students. Free solvers can also be downloaded from the inetrnet. Some possible sites are <http://www.lindo.com/> and <http://sourceforge.net/projects/lipside/>. Many more may be there.