ELEC 6270-001: Low Power Design Class Projects, Spring 2013, **Assigned 2/13/13**

1. Find the optimum voltage and power savings for various logic gates when using a level converter in CMOS 32 nm bulk technology ***(Karthik N.).***
2. Estimate power saving by clock slowdown for s5378 in 45 nm and 22 nm bulk CMOS ***(Parameshwaran G.).***
3. 32-bit ALU with sleep mode for 22 nm technology ***(Yu Wang).***
4. Power comparison of a 4 bit binary, gray encoding and one hot encoding counter designed in 22 nm CMOS ***(Philip Reiner).***
5. Gated clock 32-bit parallel load register and shift register designed in 32 nm CMOS ***(Swathi B.).***
6. Implement a divider in 32 nm CMOS with gated flip-flops and estimate power saving ***(Nikita R.).***
7. Normal speed 32-bit adder with reduced supply and parallelism in 32 nm CMOS ***(Nikhil G.).***
8. Low voltage operation of a 16 bit counter in 32 nm CMOS technology ***(Harshit G.).***
9. Design of s5378 in 32 nm CMOS for reduced scan mode activity ***(Praveen V.).***
10. Low power RF amplifier in 32 nm CMOS ***(Yuanze Li).***
11. Minimize test power for c6288 in 32 nm CMOS by optimal ordering of vectors ***(Jagadish Babu S.).***
12. Redesign control FSM of a multicycle processor with low power state encoding and estimate power savings ***(Sushma K.).***
13. Gated clock BIST circuit to test c6288 circuit in 32 nm technology ***(Sindhu G.).***
14. Effects of process variation in Vth on power dissipation for a 32-bit adder ***(Bei Zhang).***
15. Comparing parameters (I, f, P, E) for a 32 bit adder designed in NAND only gates and spectrum design in 32 nm CMOS ***(Yixuan Wu).***
16. Comparing parameters (I, f, P, E) for c5315 designed in 90 nm and 45 nm CMOS ***(Sowmya S.).***
17. Comparing parameters (I, f, P, E) for c7552 designed in 45 nm bulk and 45 nm high-k CMOS ***(Zhan Su).***
18. Redesign non-critical path gates of a 32 bit adder for slower operation and estimate power savings ***(Hechen Wang).***
19. Use a dual voltage supply to operate non-critical path gates of a 32 bit adder at a lower voltage and estimate power savings ***(Rong Jiang).***
20. Estimate power savings for c2670 with adiabatic logic design ***(Ruixin Wang).***
21. Design and compare parameters (I, f, P, E) for a 32 bit adder with CMOS NAND and CPL NAND gates ***(Dongyi Liao).***
22. Design ring oscillators of different frequencies in 32 nm CMOS for reduced voltage operation and estimate power savings ***(John Francy).***
23. Modify the Vth of the non-critical path gates of a 32 bit adder and estimate power savings ***(Jie Zou).***
24. Reducing glitch power for c5315 circuit designed in 32 nm CMOS ***(Rathan Raj).***

***Expected Results:***

1. Clear understanding of the problem.
2. A to the point analysis.
3. Reliable (reproducible) data.
4. Meaningful conclusions usable by others.
5. A readable four to six page report (**due on 4/15/13**) written and formatted like a technical paper (PDF).