Design of a Low Power 5GHz CMOS Radio Frequency – Low Noise Amplifier

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Abstract

A 5GHz low power consumption LNA has been designed here for the receiver front end using 90nm CMOS technology. The 'current reuse' technique has been used here to reuse the bias current for two amplifier stages stacked upon each other. An inverter type amplifier acts the second stage to a common source first stage thereby giving a good gain for the amplifier. The gain achieved is around 13dB with a power consumption of 4.8mW.

Key Words: Low Power, RF CMOS, LNA, 90nm, 5GHz.

1. Introduction

Power consumption is a very important criterion in wireless communication systems. At the same time we need to have a cost effective solution for the problem of constructing RF circuits using non SiGe technologies. We need a substitute that can provide the benefits of the SiGe technology like low power and high gain. This is one of the reasons why the use of the CMOS technology is increasing in the design of the Low Noise Amplifiers of the RF Front end. There are certain CMOS designs that consume several tens of milli watts, this approach reduces the power consumption to just a few milli watts.

In this work, a current reuse technique is employed to increase the transconductance of the LNA without increasing the power consumption compared to the standard cascode technology. The design comprises of a common source amplifier followed by an inverter type amplifier in a stacked up arrangement as shown in the circuit diagram in Figure 1. The PMOS-NMOS inverter type amplifier gives a major part of the gain we are looking for.

The traditional approach towards design of CMOS LNAs involves the use of multiple cascade stages to achieve the gain which results in higher power consumption because a single cascade stage consumes four to five times more current than the low power LNA design under comparison. Hence we get more power dissipation. Typical power dissipations for the cascade design for a gain of 13 – 14dB range from 8mW to 20mW [1-5]. The goal of this work is to achieve at least a fifty percent reduction in that.

2. Design of the Low Power LNA

The circuit diagram of the LNA can be found in Figure 1. The RF input is fed into the common source input stage whose input impedance is matched to the source impedance. The charactereistic impedance of the circuit is 50 Ohm and hence the source impedance is chosen to be the same. It has to be noted that the impedance matching circuits has not been shown completely just to keep things simple before begginning.

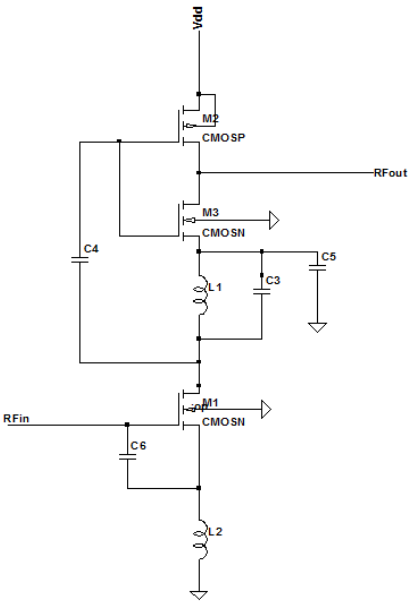

Figure 1, The LNA Circuit without matching at input and output

The amplified output of the transistor M1 is fed into the gates of the inverter type amplifier pair comprising M2 and M3 using the coupling capacitor C4. As it can be seen from Figure 1, the two stages have been stacked up between 'Vdd' and 'ground'. Which means we need an isolation between M1 and M3 and that is provided by L1 and C3. The inductor-capacitor pair resonates and causes a high impedance path between the nodes they are connected thereby giving the required isolation. Capacitor C5 acts as a bypass for the second stage. The RF output is taken from the common drain terminals of M2 and M3 transistors.

It can be seen that all the 3 transistors use the same bias current. When compared to the traditional design where multiple stages of 'cascode' amplifiers are used with each stage having a bias current, this design should consume at least fifty percent less power.

The first step towards the design of the amplifier is to find the optimum transistor widths. The transistor widths

decide the amount of bias current that will be used and hence the power consumption. For this design the width is chosen to be 20 because this width gives a good drain current density of 0.13mA per micro meter width, which is needed for an NFmin of less than 3dB and a power dissipation limit of 4mW for a supply of 1.2V.

Then we need to look into the input matching, which involves both noise matching and impedance matching. Since it is very hard to achieve both at the same time, a trade off is done between the two. We need to choose the value of 'Cgs' of M1 for noise matching such that,

$$Cgs = \frac{2Gopt}{2\pi f} \quad (1)$$

Here 'Gopt' is the optimum admittance of the source for a lower Noise Figure, here it is 1/50 or 0.02. For 5GHz we get the value of 'Cgs' to be 1.2pF. Since the transistor gate-source capacitance found through spice analysis is only 30fF we choose to add a parallel capacitance C6 of 1.2pF across the gate and the source.

Impedance matching at the input and the output are the next two things that need to be considered. For matching at the input we need to make sure that your impedance is 50. A technique called 'inductive degeneration' is used for the same, where the capacitances are cancelled out by the inductors and we are left with only 50Ohms as the input impedance. Considering the coupling capacitor C1 as well, we get an expression for the input impedance as,

$$Zin = s(L2 + L3) + \frac{1}{s(C1)} + \frac{1}{s(Cgs1)} + gm1.\frac{L2}{Cgs1} \quad (1)$$

The coupling capacitor C1 is chosen as 1pF, L2 is chosen such that the last term gives us exactly 50Ohms and also to cancel out the capacitance Cgs. L3 does the job of cancelling out the impedance of C1. L2 needs to be small enough to be implemented as a spiral inductor and hence it is chosen at around 1nH or less. Gm1 is the transconductance of transistor M1. A similar calculation is done for the output impedance and it is found to be given by the expression,

$$Zout = \frac{1}{s(Cds2)} + \frac{1}{s(Cds3)} + \frac{1}{cC2} + gm3.\frac{L1}{Cds3} \quad (2)$$

Cds2 and Cds3 are the drain to source capacitance of M2 and M3 and Gm3 is the transconductance of M3, found through spice simulation. L1 is used for the isolation that we talked about between the two amplifier stages.

After calculating the input and output matching circuits using the above expressions we get a circuit shown in 'Figure 2'. L1 and C3 are chosen to resonate at 5GHz and C5 acts as a bypass capacitor for the source of M3. C3 and the coupling capacitor C4 are chosen to be 1pF to aid in the calculations. Since we cannot use inductive degeneration for the output of the second stage, a matching circuitry comprising of C8 and L4 will give the necessary matching of 50Ohms at the output side.

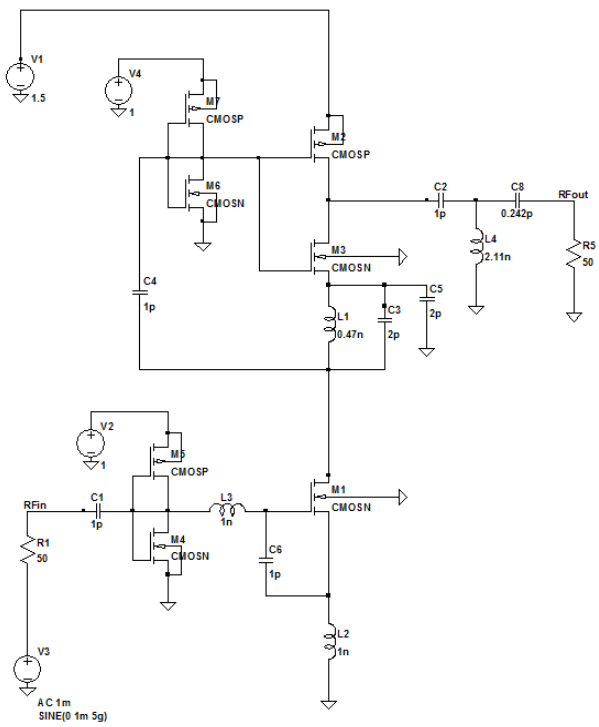

Figure 2, same circuit as in Figure 1 but with input and output matching circuits and input biasing.

The biasing circuitry also needs to be added as we need to bias the two stages at exactly the center of the slope on the transfer characteristics of that stage. M5 and M4 are small transistors which are of widths 0.09um and 0.036um respectively chosen such that a bias of 0.5 volts is applied to the gate of the transistor M1. These transistors consume very little power compared to the main amplification stages. A similar job is done for the second stage with M7 and M6 for a bias point of 0.35 volts. These voltages are determined by sweeping the input of the transistor stages and evaluating the transfer characteristics using spice.

The circuit is simulated using spice tools like HSPICE and the circuit 'S parameters', 'Noise Figure', 'NFmin' and 'power' are measured by analyzing the plots. The circuit should essentially consume lower power but one of the demerits of this design comes because of the fact that the bandwidth is smaller compared to the cascode approach as we use a resonating circuit between the two stages which limits a huge chunk of frequencies. So it results in a good design but more of a tuned circuit and more suitable for RF applications that use such tuned circuits. The circuit parameter values and the results are analyzed in the next section. The gain that it is calculated

using small signal models of the stages is around 12dB with a power consumption of 4mW.

3. Analysis of the results

The parameters of the circuit are analyzed with respect to the frequency of operation and their behavior outside and around the 5GHz frequency. Since the circuit comprises of a lot of reactive elements, we get abrupt changes around the operating frequency and this is what is expected.

A plot of the S parameters is shown from Figure 3 to Figure 5. The S21 plot is of importance as it gives the gain of the amplifier. As it can be seen from Figure 3, a gain of 13dB is obtained at 5GHz which falls right in our desired range.

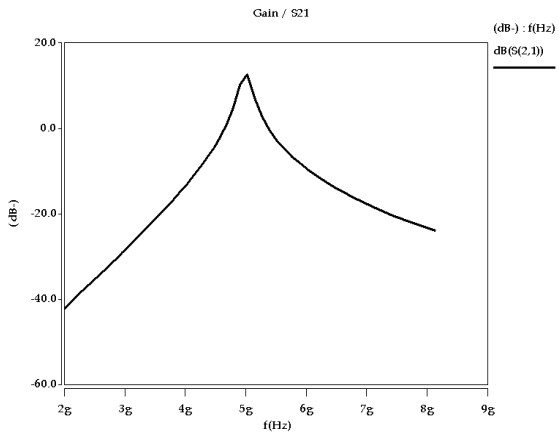

Figure 3, a plot of the power gain of the circuit versus frequency

Figure 4 shows a plot of the input and output reflection coefficients S11 and S22. The values are -10.3 dB and -14.5dB respectively for the input and output sides. The negative value of S11 indicates that a good matching has been provided at both the input and the output.

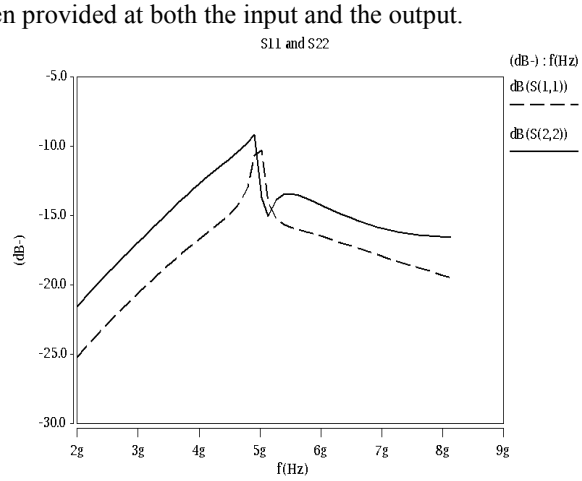

Figure 4, a plot of input and output reflection coefficients S11 and S22.

Figure 5 gives the plot of the reverse isolation or S12 that is provided by the circuit. The value of the isolation that was got is -45.86dB which is very good figure. This is attributed to the resonating circuit that is inserted between the two stages.

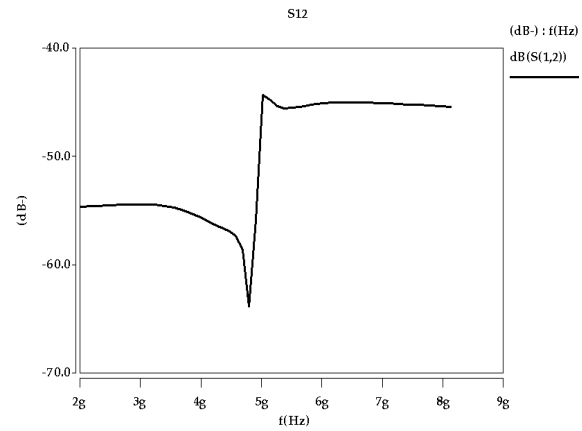

Figure 5, Reverse Isolation S12

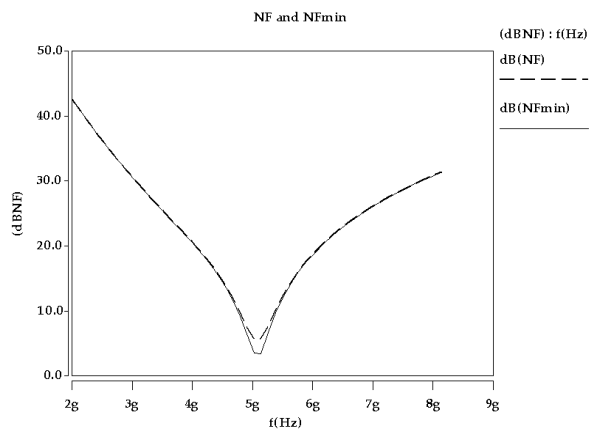

Figure 6, Noise Figure and NFmin plot

The plots of Noise Figure and NFmin are shown in the Figure 6 here. A NF of 5.6dB is obtained with the NFmin being 3.5dB. Input noise matching is the most probable reason for the NF to have exceeded our expectations. The expression for NF is given by [6],

$$NF = NFmin + \frac{Rn\{(Gs-Gopt)^2-(Bs-Bopt)^2\}}{Gs} \qquad (3)$$

Here, NFmin directly depends on the amount of current biasing we provide for the circuit. Since we had a limit of the amount of current that can be used for biasing because of the power constraints the current could was chosen to give us a small NFmin. The NF also depends on the noise matching at the input port which again is given by the second term in the above expression for NF. 'Gs + jBs' is the source admittance presented to the transistor M1 and

'Gopt + jBopt' is the optimum source admittance [6] and both need to be equal to get a good noise match. This calls for a tradeoff between impedance matching and noise matching as they never result in the same values for the matching circuits and hence both are not possible at the same time. Even though 'Cgs' was enhanced for noise matching as explained in the design, the addition of C1 as an input coupler has resulted in a noise mismatch and hence a value of NF that is high compared to the results in [1-5].

The power is the main consideration here and power measurements yielded 4.8mW power consumption. It is calculated by multiplying the supply voltage with the bias current which was found through simulation to be around 3.2mA. This is comparable to other low power designs and also when compared to the conventional cascode designs a good power saving of more than 40 percent is achieved [4, 5]. The supply was slightly increased to get a better gain and NFmin and hence the power dissipation went out of our desired range of 4mW.

The results are summarized and compared to other related works in the area of low power LNA design and also with some designs employing the cascode strategy. The results are tabulated in tables 1 and 2.

parameter	[1]	[2]	This work
Technology (nm)	250	90	90
Voltage Supply (V)	2	1.2	1.5
Frequency (GHz)	2.4	5.5	5.0
Gain (dB)	14.7	15.4	13
Noise Figure(dB)	2.5	2.7	5.6
Power (mW)	1.97	20.6	4.8
S12 (dB)	-28	-32	-45.86
S11 (dB)	-20	-14	-10.3
S22 (dB)	-22	-8.8	-14.5

Table 1, comparison of this work with other low power LNA designs

4. Conclusions and Future work

An RF LNA is designed here using CMOS 90nm technology for low power operation with a current reuse technique for biasing. The bias current is shared between the two transistor stages and a method for feeding the signal from the first stage to second stage using parallel resonance for isolation of the drain and source regions of the transistors in the two different stages is employed. This is different from the conventional cascode approach where multiple cascode stages or a single cascode stage with more current bias is used resulting in more power consumption.

parameter	[3]	[4]	This work
Technology (nm)	90	90	90
Voltage Supply (V)	1.2	1.2	1.5
Frequency (GHz)	5.5	3.1 – 5.9	5.0
Gain (dB)	13.3	13.5	13
Noise Figure(dB)	2.9	2.8-3.8	5.6
Power (mW)	9.72	5.4	4.8
S12 (dB)	-28	<-57	-45.86
S11 (dB)	-14.4	~-15	-10.3
S22 (dB)	-19	NA	-14.5

Table 2, comparison of this work with some cascode designs

As a part of the future work the noise matching of the circuit can be improved by understanding the concept of matching the optimum noise admittance of the source to the actual source admittance and its relation to the input impedance of the circuit.

The power supply voltage and the voltage needed to keep the transistors in saturation usually limit the number transistors that can be stacked up. An analysis of optimum number of transistor stages that can be used to receive a good gain can be done. This would enable us to understand the limit for a particular supply voltage. If we can have more stages stacked for the same supply, we will get a huge gain compared to the cascode design with lesser power consumption.

One of the most basic things about an amplifier that was clearly visible in this design and simulation is that when we supply more DC power to the circuit through an increase in the Vdd and bias current, we get more gain. So during the design for low power of an amplifier, the entire power supplied is not injected into the signal, some quantity gets dissipated or lost as heat. We just need to utilize this lost power such that a larger percentage of supplied power is converted into gain.

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