

Design of a New Low-Power 2.4 GHz CMOS LNA

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(Received 11 February 2001)

A 2.4-GHz single-stage CMOS low noise amplifier (LNA) structure with ultra low power consumption is proposed. A current reuse technique is used to decrease power dissipation with increasing amplifier transconductance for the LNA. Thus, the same amplifier transconductance for the LNA will be achieved at decreased power dissipation. Also, due to the use of an inverter-type amplifier which has a symmetric structure, the proposed LNA has high linearity. The designed 2.4-GHz LNA using 0.25- μm CMOS technology achieves a power gain of 14.7 dB, a noise figure of 2.5 dB, and an IIP3 of 0.5 dBm even at a power consumption of 1.97 mW.

PACS numbers: 84.40.Dc

I. INTRODUCTION

CMOS integrated circuit for wireless applications in the 2.4 GHz frequency range are receiving much attention due to their potential for low cost and the prospect of system on a chip integration, although bipolar and GaAs are currently the preferred technology [1,2]. Power consumption is very important in wireless communication system. However, the low-noise amplifier (LNA), which is a key building block for the RF front-end of the receiver, typically has high power consumption. While recent works have demonstrated the potential of CMOS LNAs, they generally have difficulty in attaining low power consumption to meet the required specifications. Previous CMOS LNAs have had a typical power consumption of several tens of milliwatts [3–6].

In this work, we propose a new CMOS LNA structure which meets the requirement of typical performance with ultra low power consumption. A current reuse technique is applied to increase the amplifier transconductance for the LNA without increasing the power dissipation, compared to standard technology. Thus, the same amplifier transconductance for the LNA will be achieved at decreased power dissipation. Also, due to the use of an inverter-type amplifier which has a symmetric structure, the proposed LNA has high linearity.

II. DESIGN OF THE LNA

Figure 1 shows a schematic of the proposed CMOS low-noise amplifier. The structure is a single-stage

LNA with inductive degeneration at the source. In this topology, a current reuse method is applied to achieve a high transconductance with less current. M_1 operates as a common-source stage, and M_2 and M_3 operate as inverter-type amplifier stages. However, they share the same bias current. The signal amplified by M_1 is coupled to the gate of M_2 by C_1 while the source of M_2 is bypassed by C_2 . The circuit thus saves power through the reuse of the bias current, so a single stage has sufficient power gain with minimized low power dissipation. Also, it is possible to achieve high forward gain and low reverse gain. Low reverse gain is desired to provide sufficient isolation and to simplify input and output matching. Also,

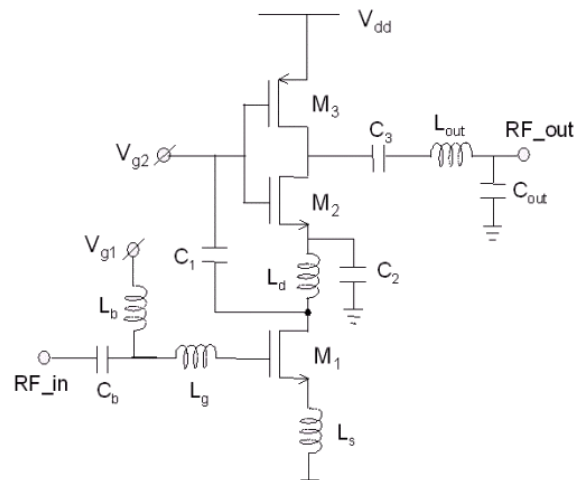


Fig. 1. Proposed CMOS LNA circuit diagram. M_1 operates as a common-source stage, and M_2 and M_3 operate as inverter-type amplifier stages. They share the same bias current.

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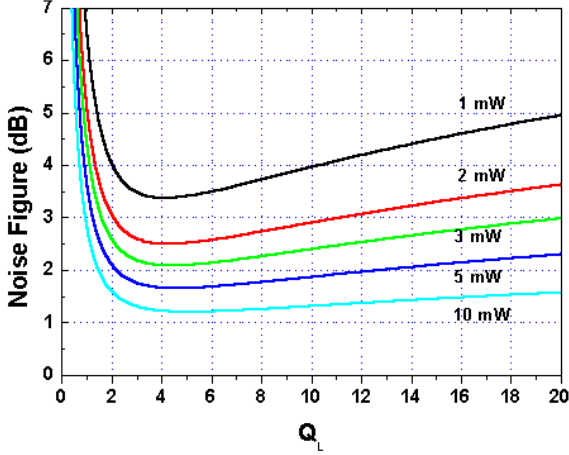


Fig. 2. Theoretical prediction of the noise figure for several power dissipations. An optimum Q_L of 4.5 is obtained.

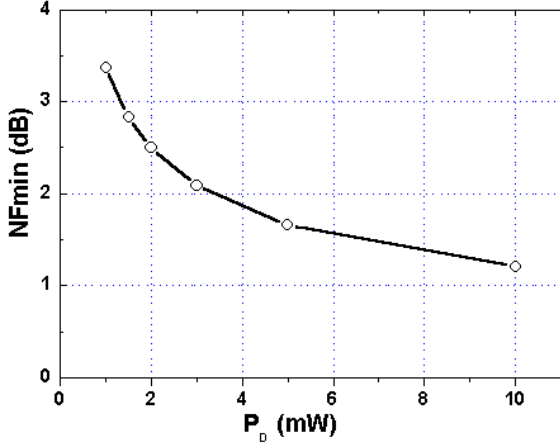


Fig. 3. Theoretical prediction of the minimum noise figure (NF_{\min}) versus power dissipation.

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega}{\omega_T} \right)^2 \left\{ 1 + 2\sqrt{\frac{\delta\alpha^2}{5\gamma}} Q_L |c| + \frac{\delta\alpha^2}{5\gamma} [1 + Q_L^2] \right\}, \quad (4)$$

$$zQ_L = \frac{\omega_o(L_s + L_g)}{R_s} = \frac{1}{\omega_o C_{gs1} R_s}, \quad (5)$$

where γ is $2/3$ in the long channel theory and it is higher than $2/3$ in the sub-micron technology. C_{gs1} can be written as $\frac{2}{3}W_1L_1C_{ox}$. The noise figure (NF) prediction versus quality factor Q_L for several power dissipations are shown in Fig. 2. The minimum noise figure exists for a particular Q_L , as shown in Fig. 2. To reduce the effects of induced-gate noise, Q_L cannot be made arbitrarily large. Additionally, a large Q_L will result in a large value for L_g , which can cause input matching variances

an inverter-type LNA shows better linearity when a symmetric structure is used. The bias voltage, V_{g2} , is set to enable the symmetric operating point so that the PMOS and the NMOS networks have the largest dynamic range. The input device M_1 is biased through bias tee of L_b and C_b . L_d is implemented as an on-chip spiral inductor. L_{out} and C_{out} are used for output matching.

The use of inductive degeneration has the benefit of simultaneously achieving both input and noise matching. The series feedback in the source provides a real impedance of approximately $(g_{m1}/C_{gs1})L_s$ to the input, where L_s can be realized with a bond-wire inductor. The input impedance of M_1 is given by

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs1}} + \frac{g_{m1}L_s}{C_{gs1}} + R_g. \quad (1)$$

Inductors L_s and L_g form an impedance matching network with the gate capacitance C_{gs} of M_1 . The matching conditions to R_s give

$$L_s = \frac{(R_s - R_g)C_{gs1}}{g_{m1}}, \quad (2)$$

$$L_g = \frac{1}{\omega_o^2 C_{gs1}} - L_s, \quad (3)$$

where ω_o is the operation frequency.

To realize a gain of 15 dB at 2.4 GHz, L_s is of the order of $1 \sim 2$ nH, which is the range to be implemented as a bondwire. The input matching of the LNA, therefore, requires only one external inductor, L_g .

The size of transistor M_1 determines the optimum input noise match or, equivalently, sets the quality factor of the input matching network, Q_L . The power consumption versus noise figure has been optimized with the method described by Shaeffer and Lee [3]. The LNA noise factor and the quality factor can be written as

due to the tolerances of both L_g and the gate capacitance of M_1 . The M_1 bias current was chosen to be 1 mA, which closely follows the 2-mW power dissipation curve in Fig. 2. Thus, an optimum Q_L of 4.5 is obtained to avoid the steep slope part of the noise figure curve. The desired Q_L value gives an optimum gate width, W , of $300 \mu\text{m}$ for transistor M_1 at an input signal frequency of 2.4 GHz. The sizes of M_2 and M_3 were chosen to be the same as M_1 . Figure 3 shows a plot of the theoretical minimum noise figure versus power dissipation. In our design, power dissipation is constrained to 2 mW, and the minimum noise figure is predicted to be 2.5 dB.

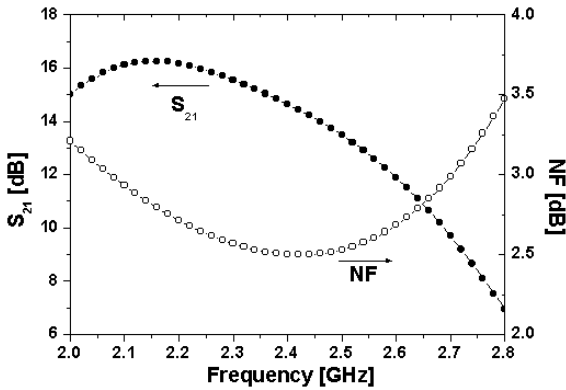


Fig. 4. Power gain (S_{21}) and noise figure (NF) of the LNA. LNA achieves a forward gain of 14.7 dB and a NF of 2.5 dB at 2.4 GHz. The power consumption is only 1.97 mW.

III. RESULTS AND DISCUSSION

The LNA is designed for a standard 0.25- μ m CMOS technology. An HP ADS was used for circuit design and simulation.

Figure 4 shows a plot of the power gain (S_{21}) and the noise figure (NF) versus frequency for the LNA. At a 2-V supply, the LNA achieves a forward gain of 14.7 dB and a NF of 2.5 dB at 2.4 GHz. The power consumption is only 1.97 mW, and a theoretical minimum noise figure of 2.5 dB is obtained. The bandpass nature of the LNA is shown in Fig. 4.

Figure 5 shows the input and the output reflection coefficients (S_{11} and S_{22}). S_{11} and S_{22} are -19.5 dB and -21.6 dB, respectively. The input and the output matchings at 2.4 GHz are very good (below -15 dB). The reverse isolation for the LNA, shown in Figure 6, is good with an isolation of more than 28 dB.

A two-tone IP3 simulation was performed on the LNA, and the results are shown in Fig. 7. The two tones were

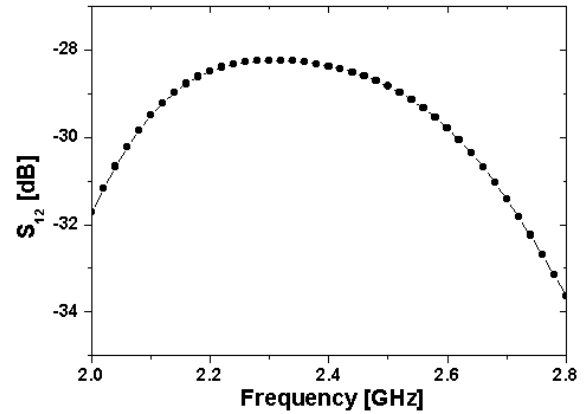


Fig. 6. Reverse isolation (S_{12}) of the LNA. The reverse isolation is more than 28 dB.

applied with equal power at 1.499 GHz and 1.501 GHz. The magnitude of the fundamentals and the third-order intermodulation products at the output are shown, and the obtained input-referred third-order intercept point (IIP3) is 0.5 dBm ($+15.3$ dBm output-referred). The linearity is primarily limited by the output-stage transistors M_2 and M_3 . Due to the use of an inverter-type amplifier which has a symmetric structure, the proposed LNA is very linear.

Table 1 shows a summary of the proposed 2.4 GHz CMOS LNA characteristics. Good performance of the LNA was obtained even at a very low power consumption of 1.97 mW.

IV. CONCLUSION

In this paper, we have proposed a 2.4-GHz single-stage LNA with ultra low power consumption. The LNA has been designed in a standard 0.25- μ m CMOS technology.

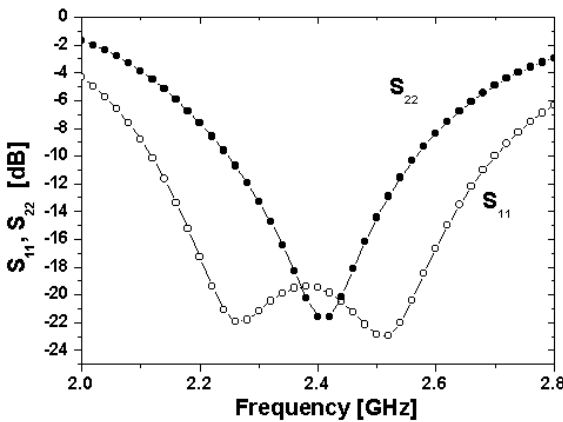


Fig. 5. Input and output reflection coefficient (S_{11} and S_{22}) of the LNA. S_{11} and S_{22} are -19.5 dB and -21.6 dB, respectively, at 2.4 GHz.

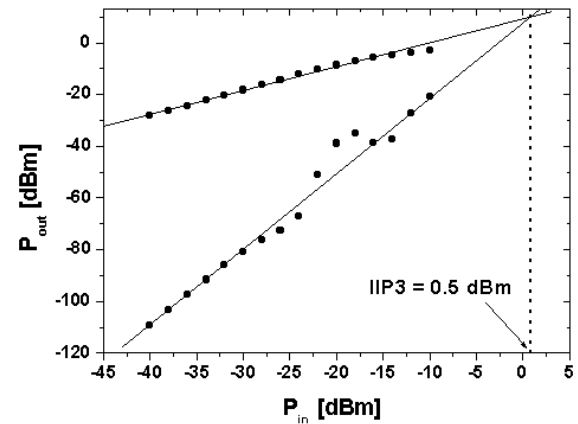


Fig. 7. LNA intermodulation product and IP3 (two-tone simulation). The obtained input-referred third-order intercept point (IIP3) is 0.5 dBm.

Table 1. Summary of the proposed LNA performance.

	Simulation results
f_o	2.4 GHz
Gain	14.7 dB
NF	2.5 dB
Power	1.97 mW
V_{dd}	2 V
IIP3	0.5 dBm
S_{12}	< -28 dB
Technology	0.25- μ m CMOS

Good noise and gain performances were obtained at a low power consumption of only 1.97 mW. A noise figure of 2.5 dB and a power gain of 14.7 dB were achieved for the proposed LNA. Also, a high IIP3 of 0.5 dBm, which shows the good linearity characteristics, was obtained.

ACKNOWLEDGMENTS

This work was supported by the Tera-level Nanodevice project of the Korea Ministry of Science and Tech-

nology (MOST) and by the Korea Science and Engineering Foundation (KOSEF) through the Micro Information and Communication Remote Object-oriented Systems (MICROS) research center at Korea Advanced Institute of Science and Technology (KAIST), Korea.

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