Report 6

ELEC 5200

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This project was all about how to use VHDL to implement a CPU. I learned about to design a CPU from scratch with the CPU basic knowledge. The interesting part and worth learning part of the design was the data interaction between the CPU, physical memory, virtual memory and cache. This made me have an overall understanding of the structure of modern computer. It helped me to refresh my memory of VHDL. This was also the most time consuming and complicate part of this project. I needed to be very careful about how each bit went through the data path in VHDL code.

For next to do this project, I would like to design a multicycle CPU rather than a single cycle CPU. Because in single cycle design, it was difficult to find a right clock cycle during simulation. And it was important to make sure each part of VHDL component working correctly before combining each part together. The single cycle CPU was to slow to implement a set of instruction respect to a multicycle CPU.

I would advise someone who starts to do this project to execute a single cycle design. Since single cycle design is much easier to build and debug than a multicycle and pipeline data path. And I would also advise to make write down note about each part of project, especially the truth table in data path design part. At last, it’s better to start each project as early as possible. You will need a lot of time to troubleshoot your VHDL design and learn to implement the memory part of this project.