Tyler Nix

ELEC 5200

Dr. Agrawal

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Part 6 Final Report

**What did you learn from this project?**

 This project gave me the opportunity to apply what I was learning in class to a real application. Breaking the design of a CPU into six, manageable pieces over the course of the semester, allowed me to focus on each step adequately to make sure I fully understood how each part contributed to the final design. This project also gave me more experience using software tools to design and, more importantly, test complex VHDL components. Overall, this project was an excellent introduction to datapath/CPU design.

**What would you do differently next time?**

 I would probably spend more time planning out my ISA, since this is the most important part of the CPU design that will either set you up for success or failure. I would also try to get to the memory module part (Part 5) quicker so that it would give me ample amount of time to figure out how to create/integrate the memory blocks into the datapath.

**What is your advice to someone who is going to work on a similar project?**

 Before you create your ISA, go through Dr. Agrawal’s slides on single cycle/multi-cycle/pipeline datapaths. The more time you spend designing the ISA and the datapath will reduce the amount of time (i.e. the number of problems) you will spend later in the project. There are a lot of resources online that are helpful as well. Single cycle datapath and single memory architecture are your friends. Also, do not wait till the last minute to start each part (especially the ISA part 1). Problems will arise, and they will take time to fix.