**CPU Project Report**

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* **What did you learn from this project?**

Firstly, we get a better understanding about architecture and operation of CPU. Secondly, in this project, we learn how to use ModelSim and Altera Quartus II IDE, which is very useful for our future study. Finally, by Combining datapath and memory on the FPGA together, it gives us a more practical understanding of FPGA board.

* **What would you do differently next time?**

In this project, we use multi-cycle to design cpu, because we think it is easy to design, in next time we will use pipeline to design.

* **What is your advice to someone who is going to work on a similar project?**

Firstly, at the beginning, student should have a background knowledge of VHDL language. Beside they need to know how to use the required software before they start the project because this will make the design more efficiency. The last advice we will give is that the debug is very boring, they need to be more patient.