ELEC 5200/6200 Compute Architecture Design
Spring 2012

Assigned 01/09/12, due 01/20/12

1. A combinational circuit compares two 2-bit positive binary integer magnitudes, A: (A1A0) and B: (B1B0), where the subscript 0 indicates the least significant bit. This circuit has three outputs—G, L and E. G = 1 if A > B, G = 0 in all other cases. L = 1 if A < B, L = 0 in all other cases. E = 1 if A = B, E = 0 in all other cases. Such a circuit is called a magnitude comparator.
	1. Write a behavior level VHDL model for the above combinational circuit
	2. Write a testbench for your VHDL model, including all possible combinations of A and B. Simulate your VHDL model using the testbench in Modelsim. Include the simulation results in your HW in wave or list format to demonstrate all these cases.
2. A rising edge-trigger 4-bit counter has a RST signal and a control signal MODE with function table specified as follows.

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| RST | MODE | Counter Function |
| 1 | X | Reset outputs to 0 |
| 0 | 0 | Count up Q+ <= Q + 1 |
| 0 | 1 | Count down Q+ <= Q - 1 |

* 1. Write a behavior level VHDL model for the above sequential circuit
	2. Write a testbench for your VHDL model, including all possible combinations of RST and MODE. Simulate your VHDL model using the testbench in Modelsim. Include the simulation results in your HW in wave or list format to demonstrate all these cases.