CPU Design Project—Part 5—Conclusions

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**What did we learn from this project?**

At the very beginning, we plan to complete this project independently. One of us is to create a multi-cycle processor with a FSM to control different clock cycles. And the most difficult part for multi-cycle processor is to adjust clock edge so that the register file and instruction register can work correctly under control signals.

 The other one is working on single cycle processor. The problem for single cycle is how to complete one instruction in one cycle the match the frequency of the hardware device. To solve this problem, we adjust the port map and simplify the component definition.

 Finally we decide to use single cycle processor.

 From doing this project, we learned about the differences between single-cycle, multi-cycle and pipelining and how they work respectively. We also realized how important teamwork is and how to assign works to make the whole team work efficiently.

**What would we do differently next time?**

We would like to try to design a pipeline processor. Since we did not fully understand how pipeline datapath worked and how to control the hazard when we began to work on this project, I thought it was too hard for me to design this type of datapath. But now, I think I can do it and in some aspects it is much simpler than single-cycle and multi-cycle datapath. And to simplify the hazard testing unit, we can just force control unit to insert several bubble or no-operation instruction for every jump and branch instructions.

**What is the advice to someone who is going to work on a similar project?**

 You should first concern about the top level design, rather than design detailed components directly. In fact every component in datapath does not work independently. Even one tiny mistake of a multiplexor can influence your datapath.