ELEC 5200/6200
Spring 2010

ModelSim Tutorial

1. Create a directory for this homework assignment.
2. Write your VHDL code in a text editor and save file as .vhd file in the directory created above.
3. The ModelSim tool is available in Lab 320 and Lab 310 computers.
4. To simulate using ModelSim, follow these steps.

STEP 1:
After starting the ModelSim, create a new project from the file menu as shown in Figure 1.
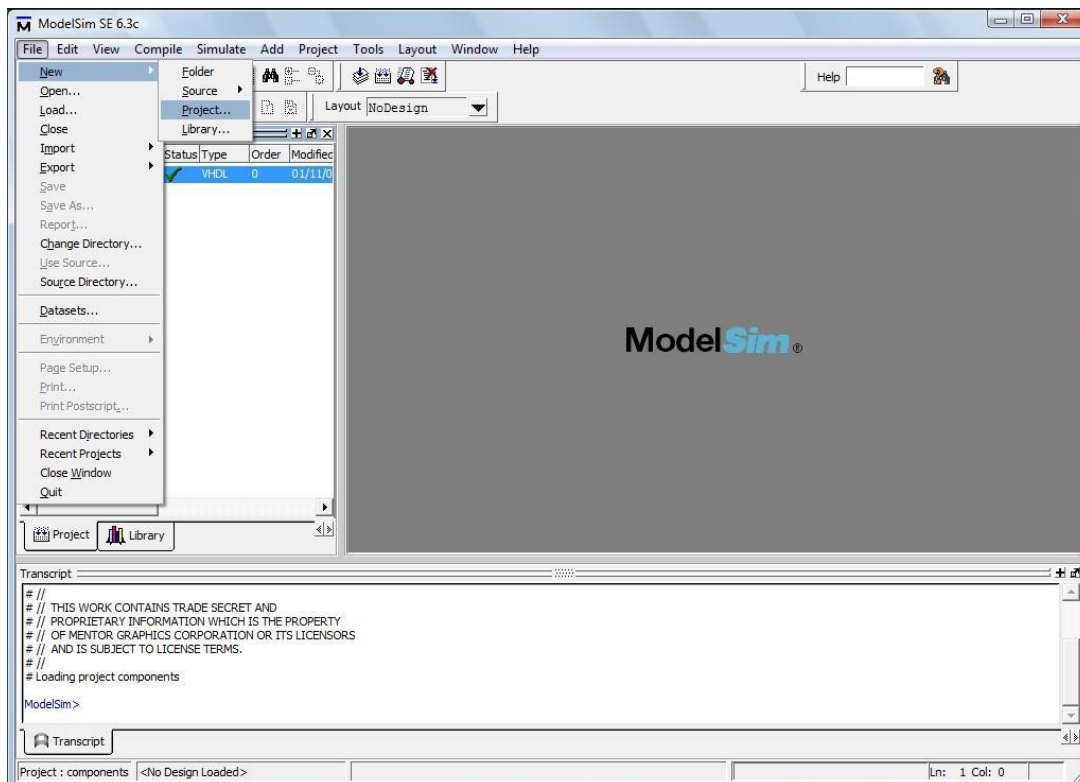

Figure 20

STEP 2:
Give Project a name. The project location is the directory in which you have your VHDL files. Click OK. (Figure 2)
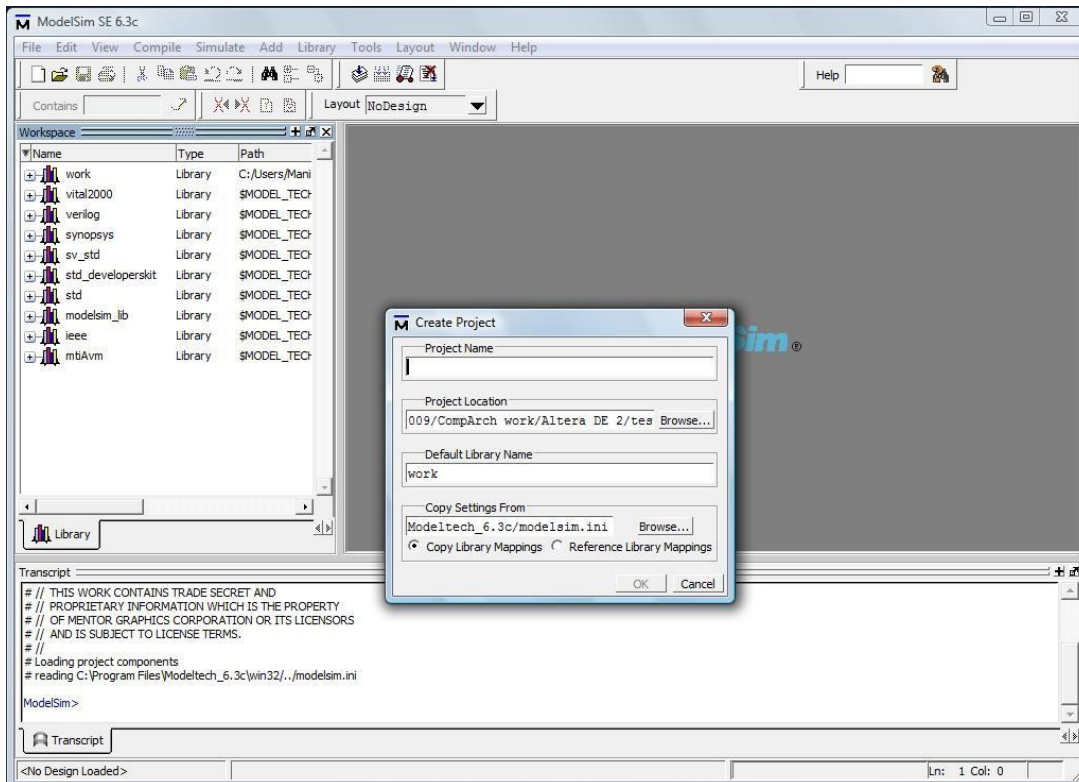
Figure 20

STEP 3:
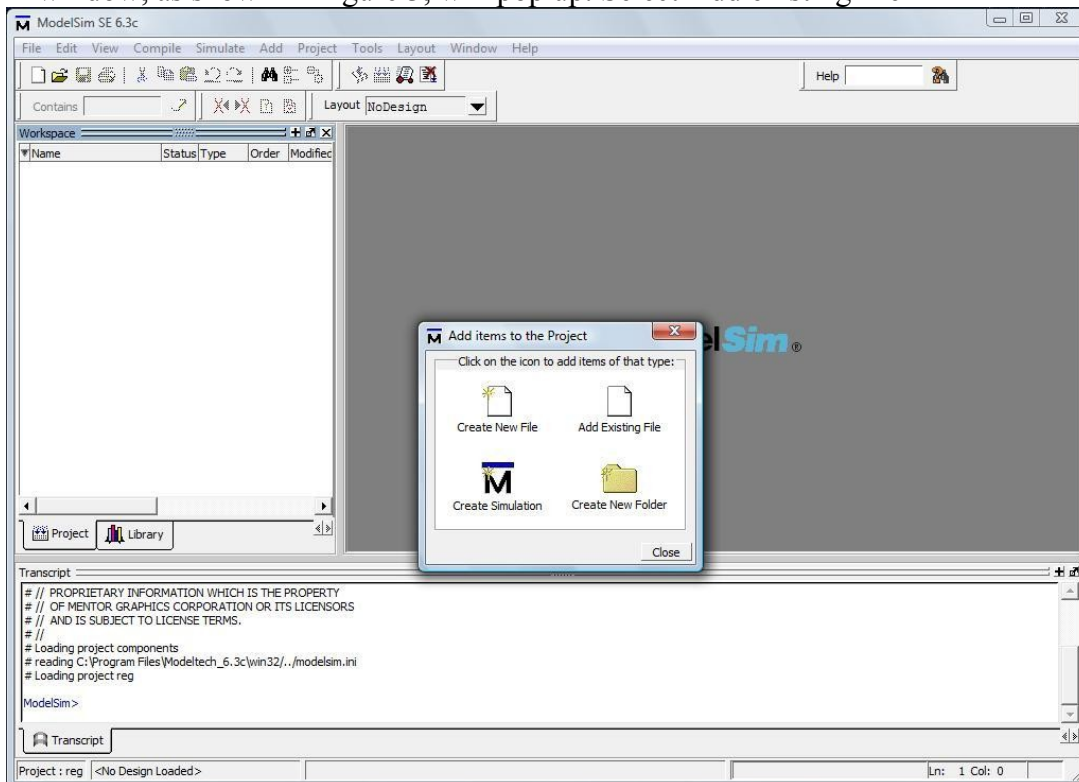A window, as shown in Figure 3, will pop up. Select Add existing file

Figure 20

STEP 4:
Brows the VHDL file of the component that you want to simulate. Make sure that you select
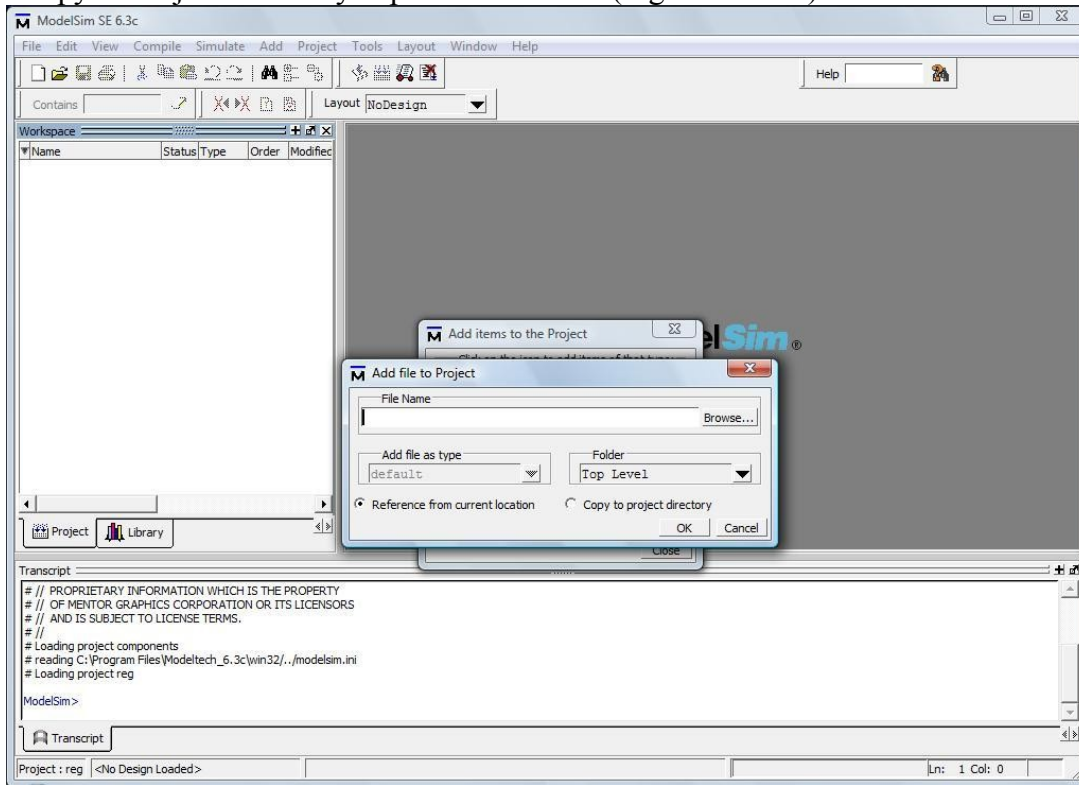"Copy to Project Directory" option. Click OK. (Figure 4 and 5)
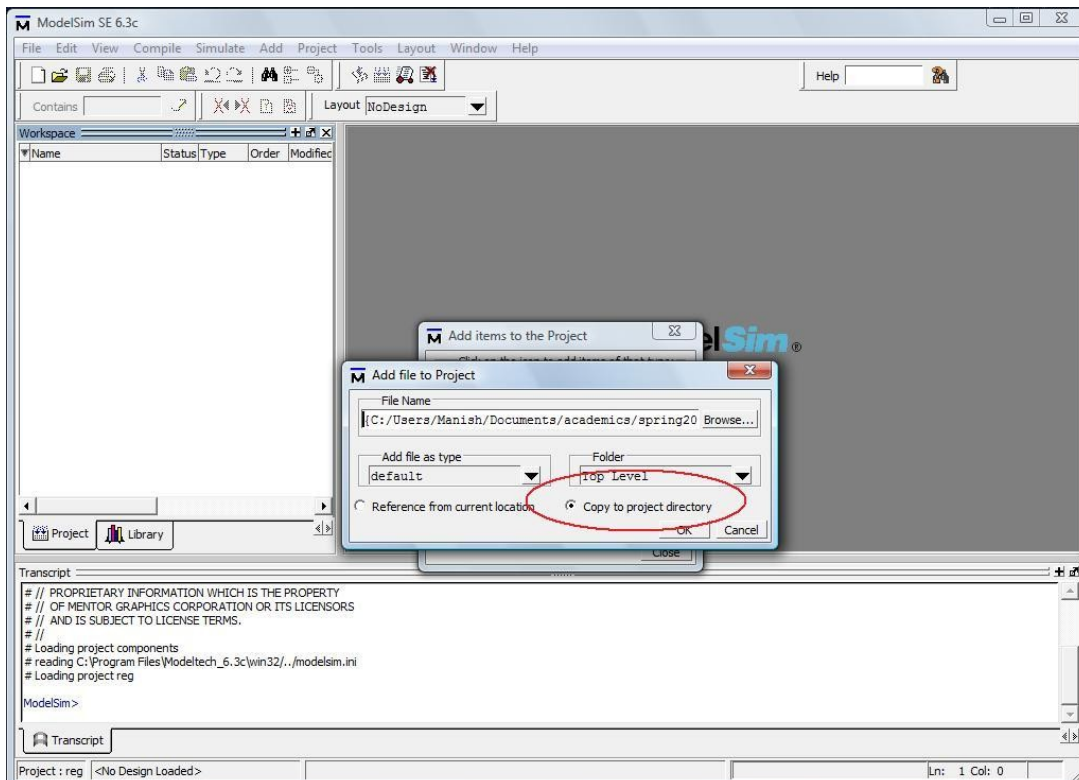

Figure 20

Figure 20

STEP 5:

The selected VHDL file will appear in the workspace as highlighted in figure 6. Double click this file to open it in the right side if the workspace.

Click the compile icon at the top as highlighted by red box in the figure 7 and the design will be compiled.
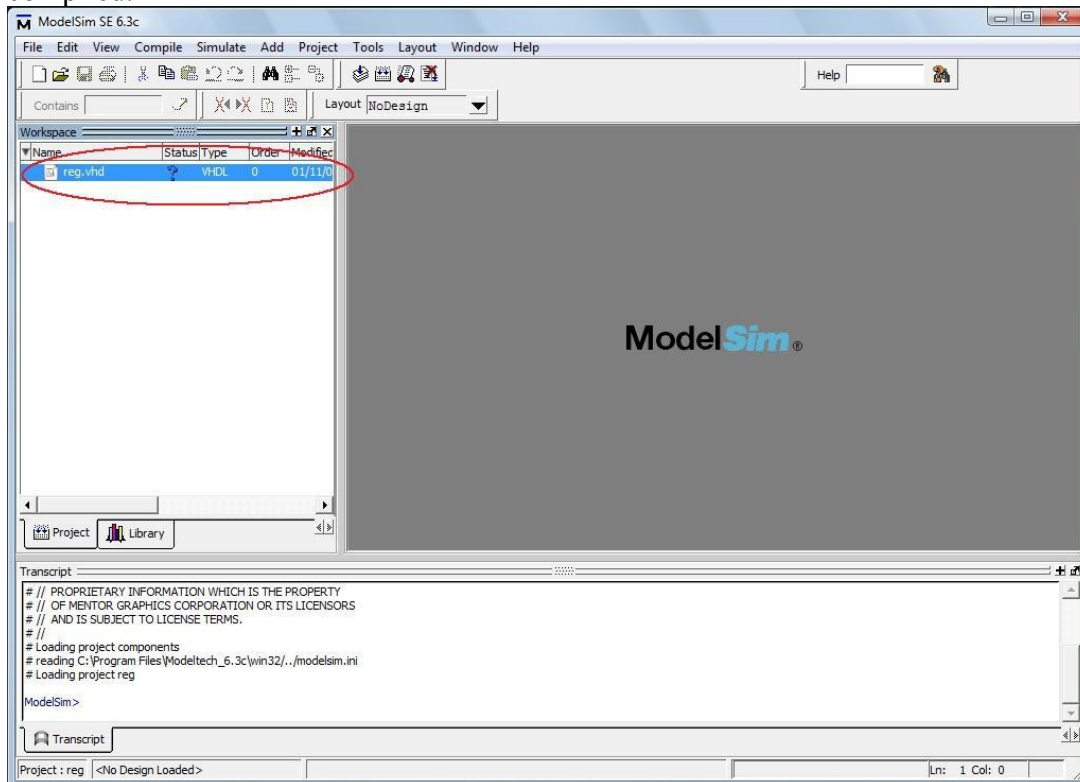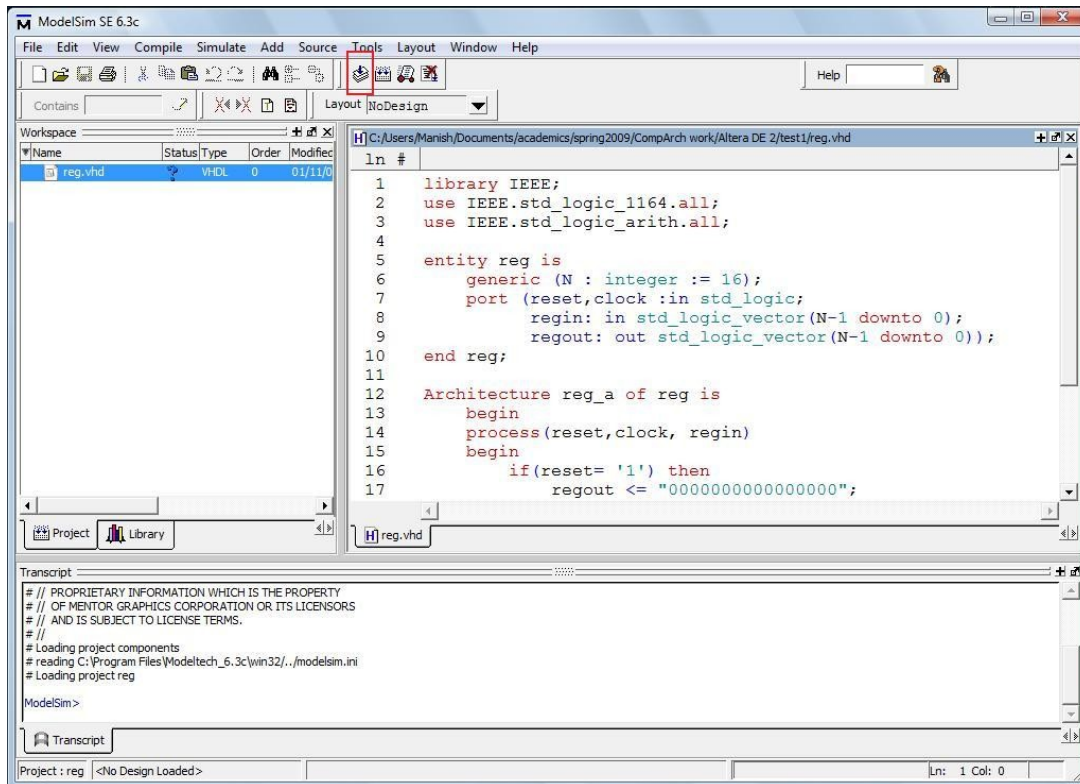

Figure 20

Figure 20

STEP 6:

If your design contains any error, the compiler will display an error message in the Transcript window as shown in Figure 8.

Double click the error message and a window will appear (Figure 9) which will contain description of the error and the line no. on which the error has occurred.

Make necessary changes in the code, save and recompile until all the errors are removed. Once all errors are removed a message will appear indicating a successful compilation as highlighted in figure 10.
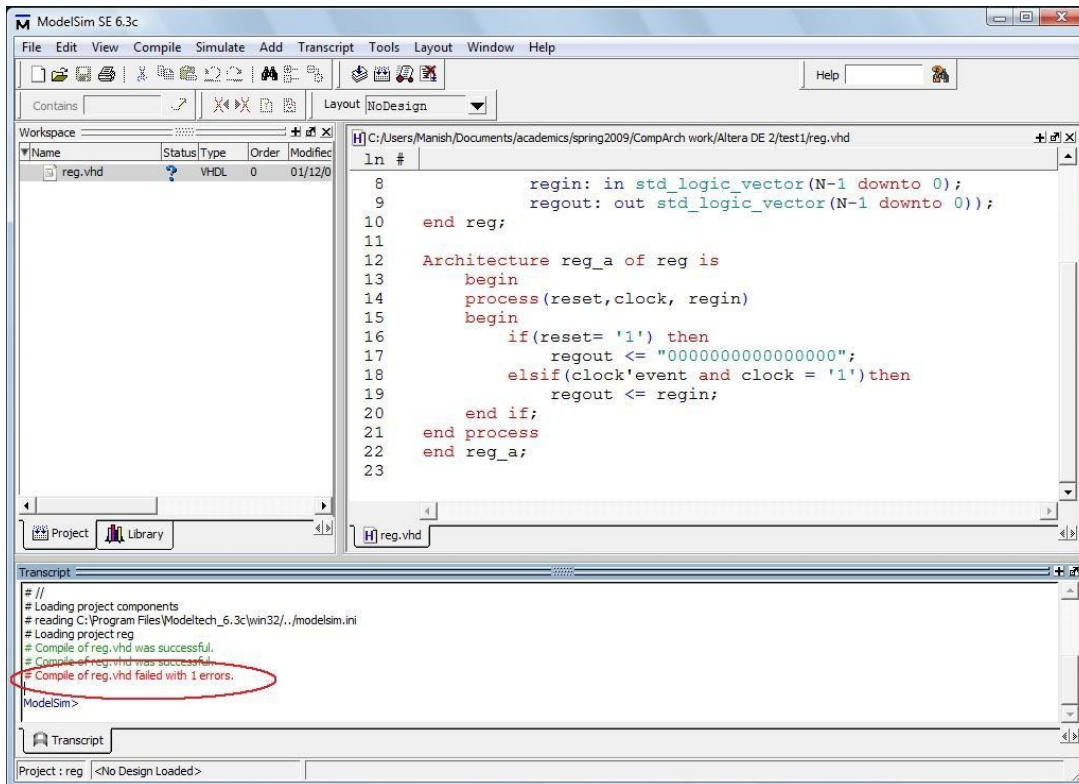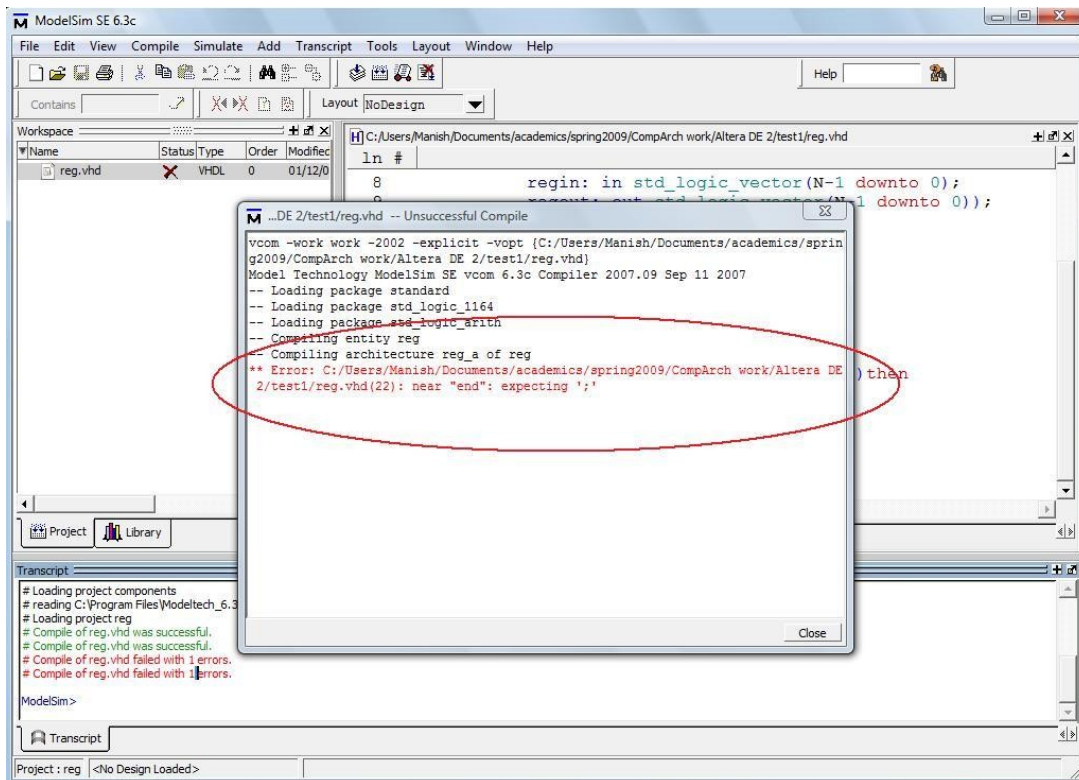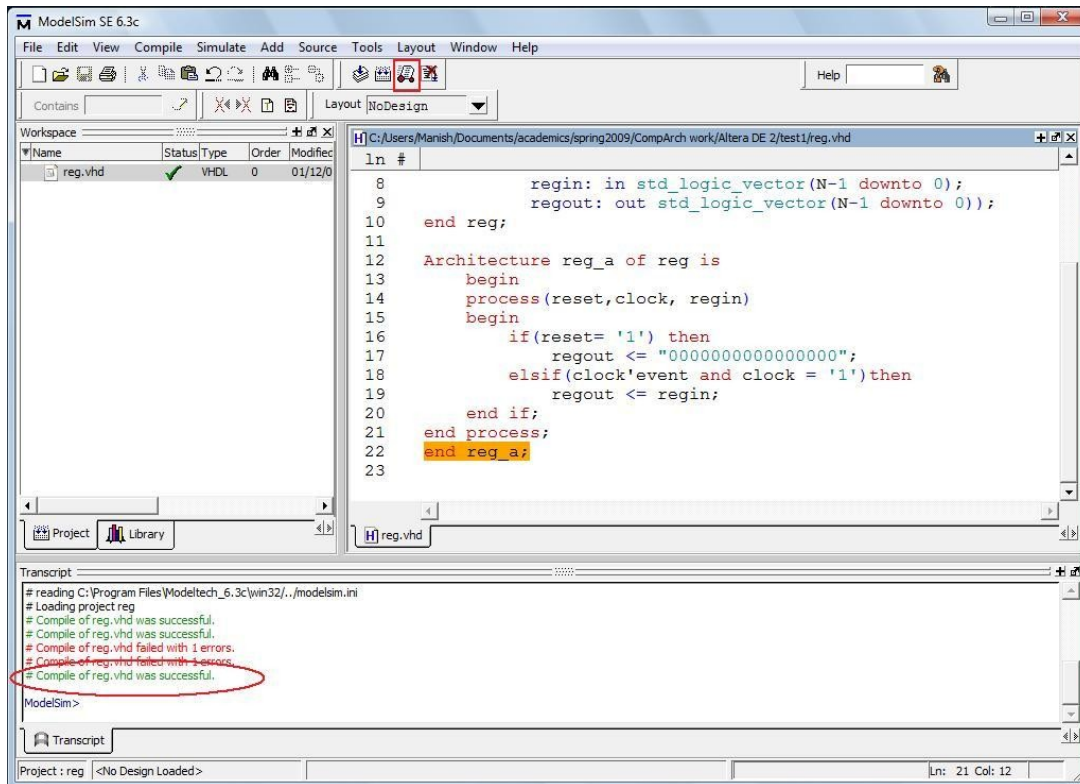
Figure 20

Figure 20

Figure 20

STEP 7:

After compilation is successful, we simulate the circuit using an icon highlighted by red box in figure 10.

A window will appear in which you will have to select the entity of component you want to simulate as shown in Figure 11.
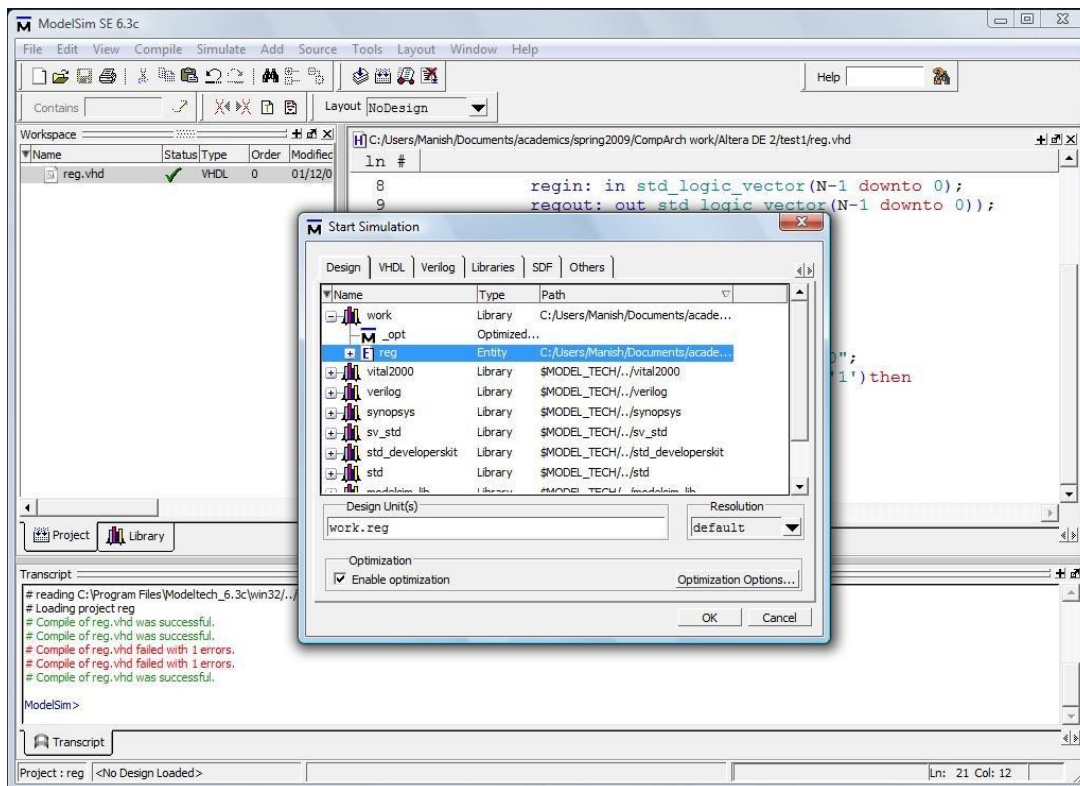
Figure 20

STEP 8:

A successful simulation will produce windows as shown in figure 12. The window at the center titled 'Objects' will contain all the input and output ports in the entity.

To see simulation results we can either use a List or a Wave. Here, the use of List is explained. A wave can be set up and used in a similar way.

To add signals in the list, right click in the Object window area and then select 'Add to List' à 'Signals in Design' (figure 12)
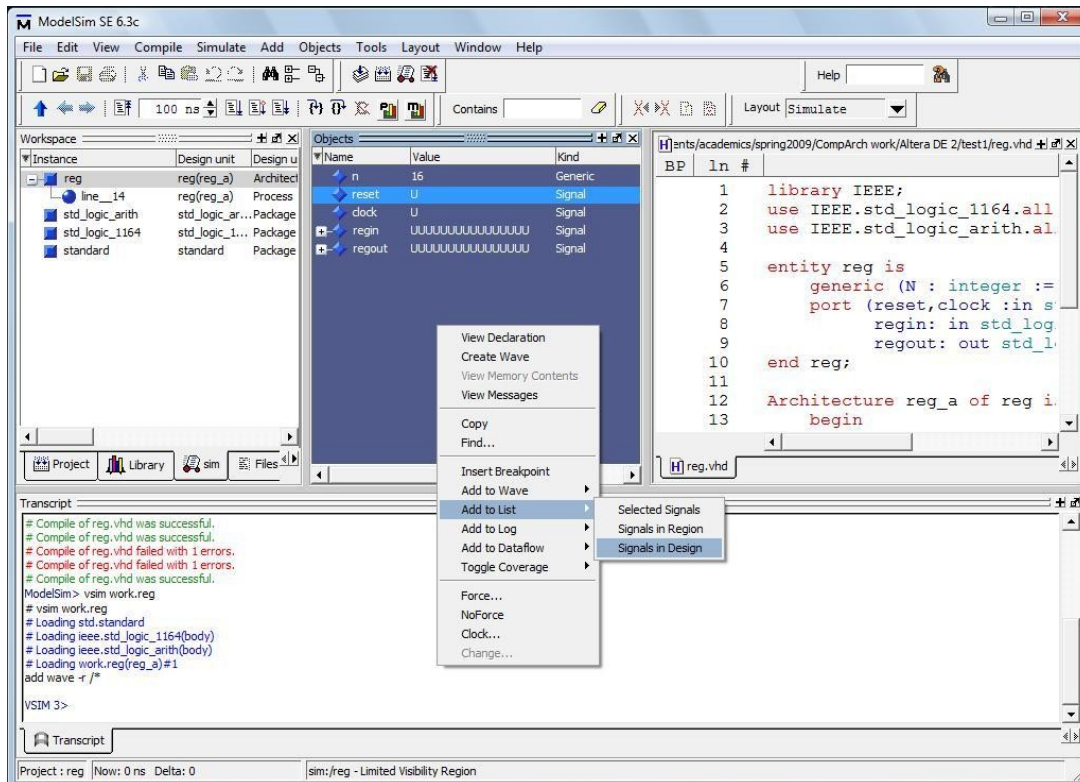
Figure 20

STEP 9:

A List window will appear to the right of Object window. Now we want to assign values to the input signal in the design. This is done by forcing the value.

To force a value to an input signal, right click on the signal and select 'force' (figure 13).

A window in figure 14 will appear. Write the value which you want to force e.g. 1 or 0 for a single bit signal or 1111000011110000 for a 16-bit vector. And click OK.
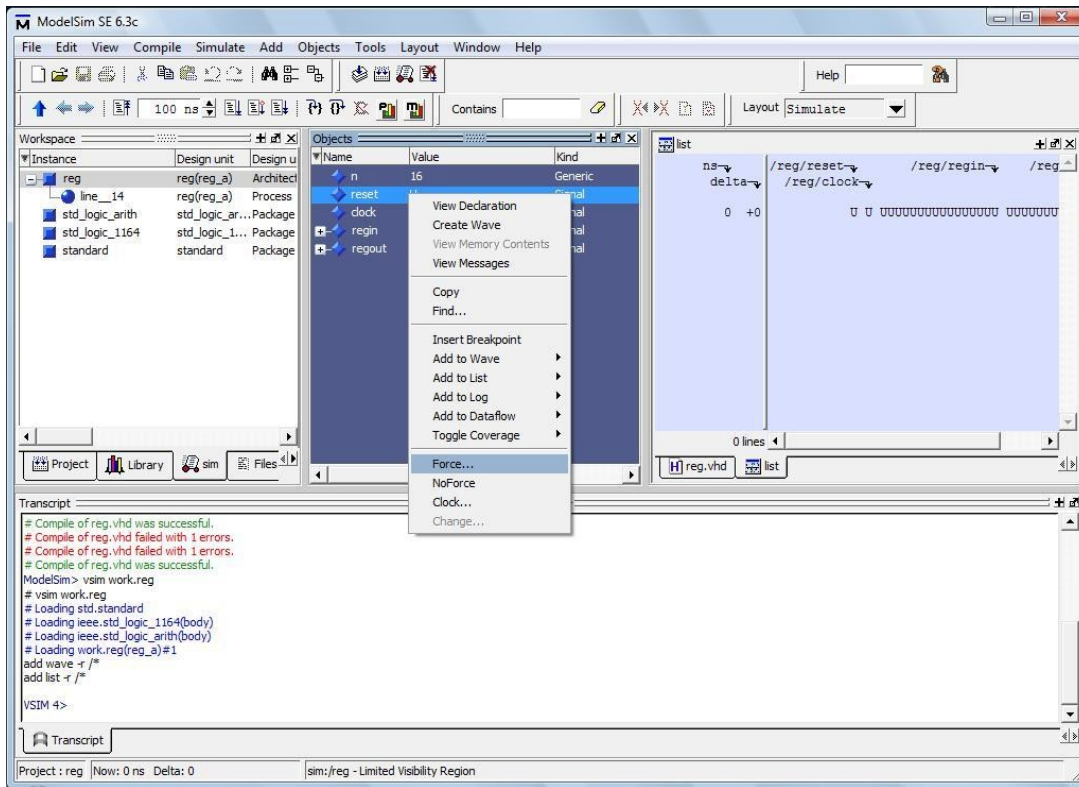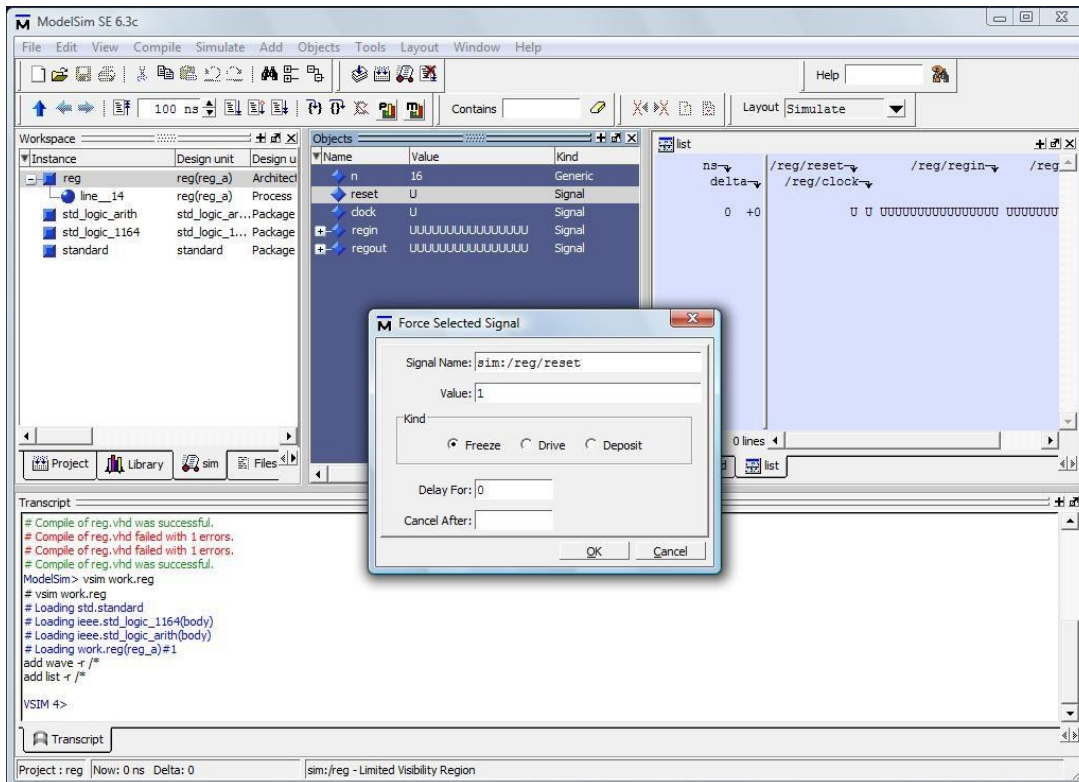
Figure 20

Figure 20

STEP 10:

If you have clock signal in the design then right click it and select 'clock' Figure 15
A window in Figure 16 will appear. You can define all the clock parameters here. Click OK.
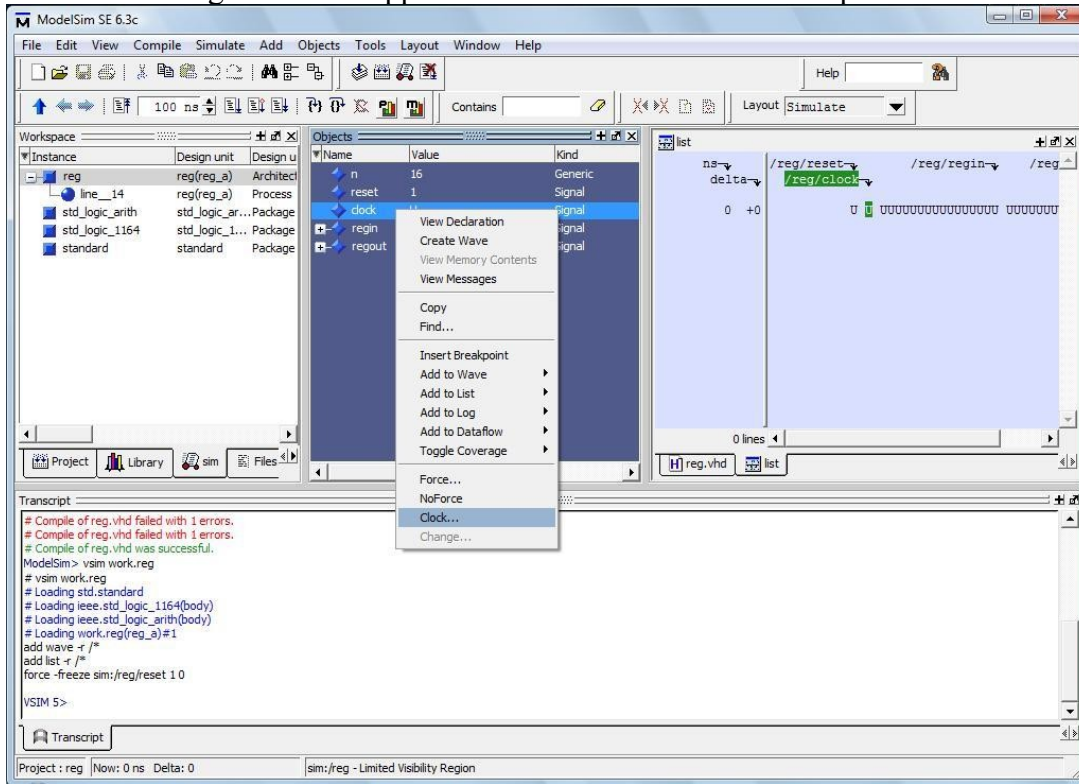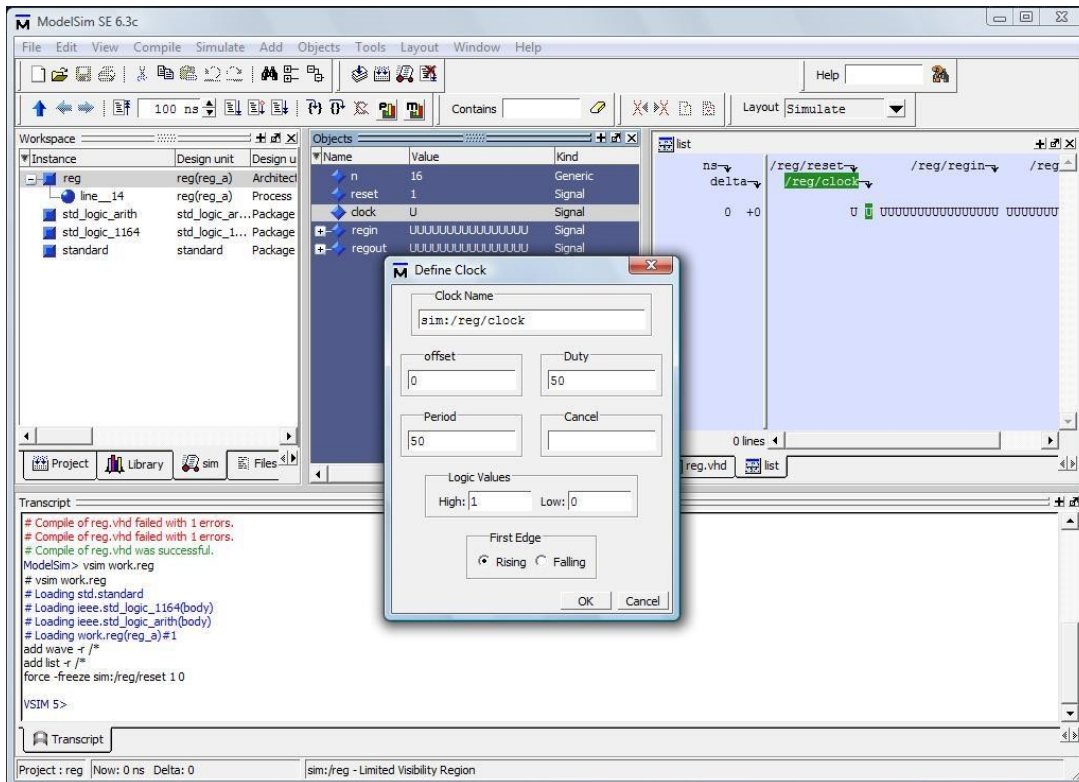

Figure 20

Figure 20

STEP 11:

Once all the input signals are assigned a value, we are ready to simulate. You can select total run time for the simulation at the as highlighted by a red ellipse. (figure 17)
Run the simulation by clicking on the icon to right of total run time as highlighted by red box. (figure 17)
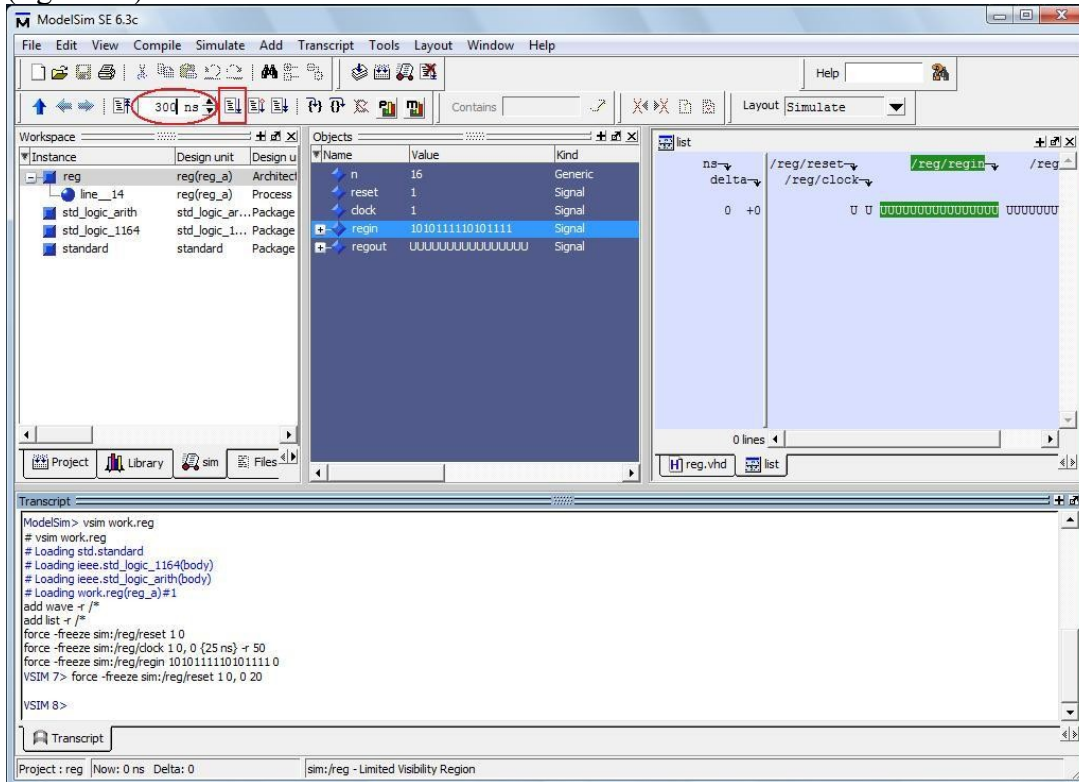

Figure 20

STEP 12:

As shown in figure 18, the list file will now contain the values of input and output signals at every time instant. This window is too small to examine the output. You can pop it out by clicking the icon highlighted by red box in figure 18.
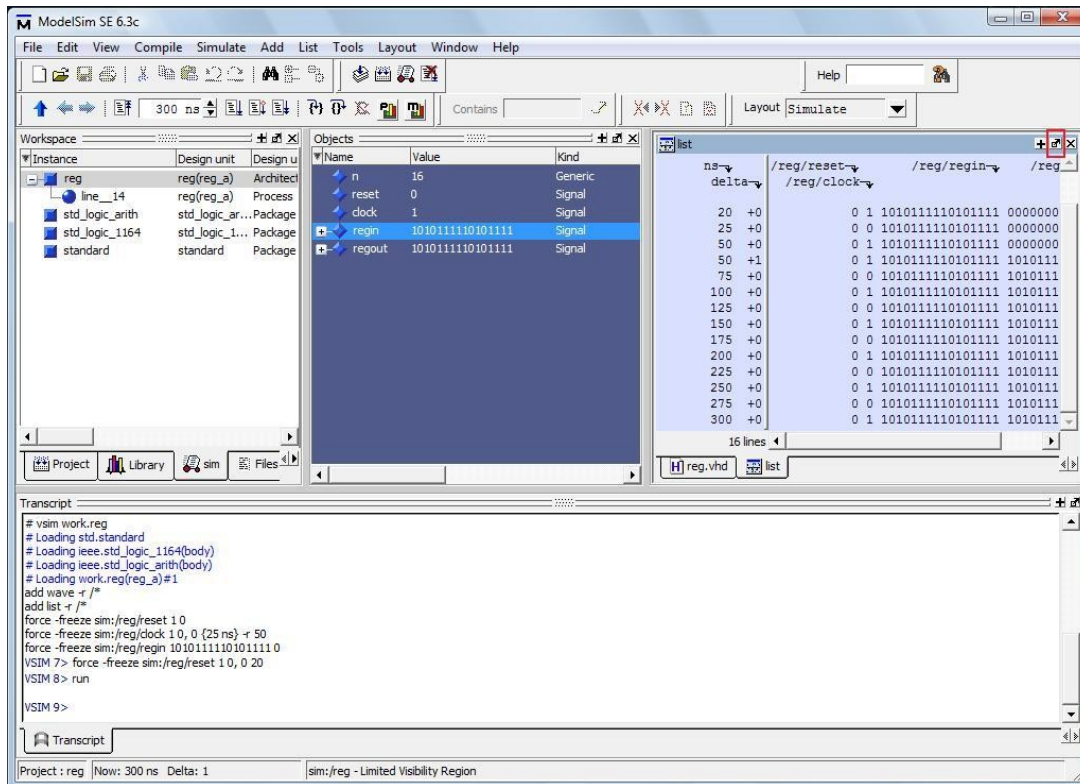
Figure 20

STEP 13:

After verification, you can save this list output as a file. To do this, From File menu, select 'Write List' à'Tabular' (Figure 19)

A window in Figure 20 will appear. Give a suitable name to your list file and Save. The Default location will be your project directory.

You can later open this file in TextPad, Copy its contents and Paste in Microsoft word.
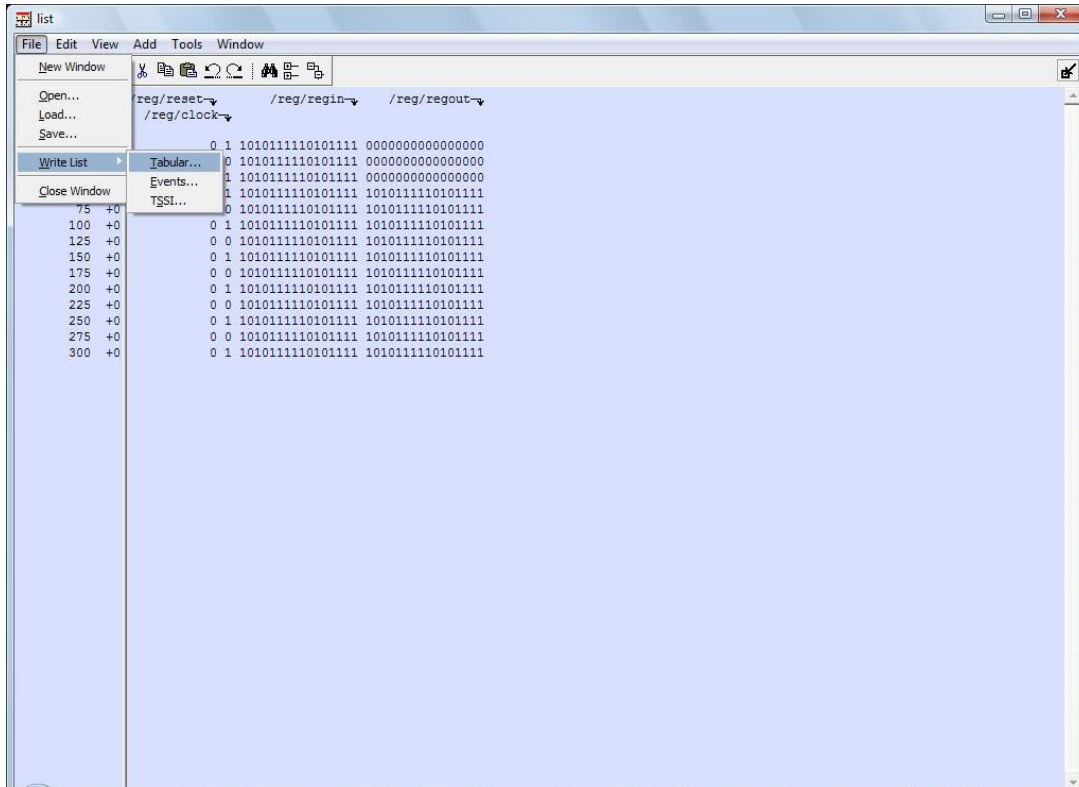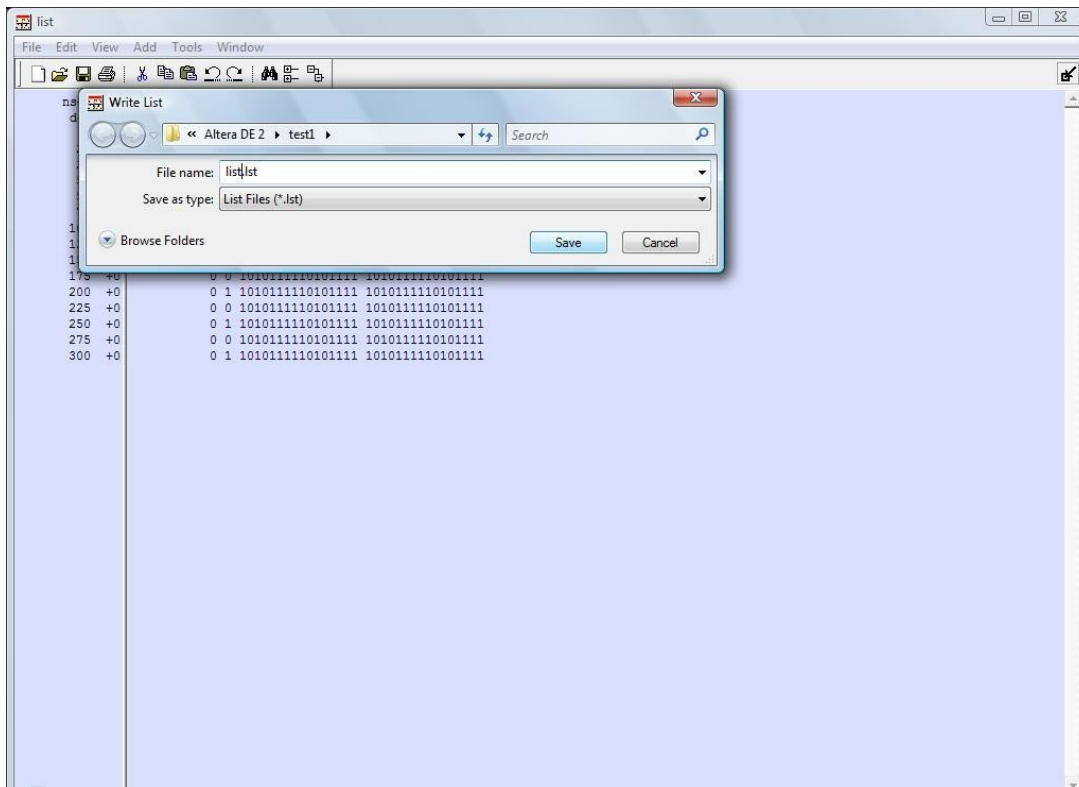
Figure 20

Figure 20