Tong Wu

ELEC 6200

Project report

Through the project, I have a better understanding on how a CPU works and how hardware and software work together. Project is done step by step, including ISA design, datapath design, construction of VHDL model, simulation and the final demo. Sometimes the previous part is revised when the latter part is designed. I think it’s very normal because I realize some faults and adjustments only after the next part is considered. I try to learn and follow what is given in the class. I think the knowledge in the class is very helpful to the project and my design is based on that materials. Changes are made because the requirement of the project is different from what we discuss in class. For example, the instructions are encoded using one 16-bit word rather than 32-bit word. I also learn much about VHDL and how to use MODELSIM simulator. The simulation and demo are very time-consuming. I have to find the reasons when the results shown are not correct. As for the demo, it seems that the software installed in LAB 320 is not compatible with ALTREA DE2 board. The memory can’t be changed by the program. That is why I don’t show the demo.

While working on it next time, I would try some other instructions. I cut off the instructions like adding value in a register with immediate for simplicity. When a register requires to be added with a number, that number must be written into another register by “mov” instruction. This behavior simplifies the design of datapath and control unit, but makes more instructions in the program. I also want to implement other instructions such as arithmetic shift. Another change I want to try is to design a different datapath. Multicycle datapath is used in my design. Pipelining is more efficient than multicycle datapath. But I don’t know much about pipelining when datapath design is assigned. In pipelining, hazards detection should be considered, and I think it would be challenging.

The first advice I give is to work in team. I finish the project only by myself rather than working in a team containing three or four students. The process of design, simulation and writing report is pretty time-consuming. It takes me much time to finish each part alone. If it is done by a team, the work can be separated into several parts, and each student is responsible for one part. The project may be done more efficiently in that way. The second advice is to be patient, especially on simulations and working on demo. We can’t guarantee that the design is perfect without faults before simulation. So when the result is not correct, or some errors occur when the VHDL code is compiled, be patient and calm down. Reading guideline of VHDL carefully before writing VHDL code may help reducing errors in the code and saving time on simulation. Finally, we should pay attention to reset signals and “halt” instruction, making sure that all the registers remain unchanged.