**CPU Design Project – Part 6**

**Mengwei zhao**

**Sihan Tao**

**Xiangyu Zhang**

1. **What did you learn from this project?**

By doing this project, we learned that how to design a CPU. It is a good experience for students to use the knowledge which learned from the course to do this project. From the first part, we need to design our instruction set architecture for a new 16-bit microprocessor that help us understand deeply about ISA. Then, we learned the architecture about the different types of datapath and its components and control signals to design a multi-cycle datapath. After that, we learned the VHDL to write codes designing the every part of CPU and modelsim software to do simulation. Finally, we learned how to simulate our processor on the Altera FPGA board provided in the lab and how to use the In-System Memory tools to run our test program straight from the Quartus software.

1. **What would you do differently next time?**

First thing I would like to do differently next time is to try a different type of datapath. At beginning, our team chose multicycle datapath, however, after learning pipeline, we realize that pipeline would be more efficient than multi-cycle datapath. Although pipeline would make this project more complicated (e.g. data hazard), it also has many advantage that singlecycle and multicycle datapath does not have. Beside of this, due to lack of experience, our part 1 (ISA) has some problems, even though we try to fix these problem during the next parts, our first part got really poor grade and influenced the next several parts.

1. **What is your advice to someone who is going to work on a similar project?**

Reviewing your VHDL ahead of time. Designing the ISA and Datapath is pretty easy since the MIPS ISA and datapath will likely be similar to yours. Get familiar with ModelSim. Know how to compile and simulate in ModelSim. Avoid Quartus II completely until you are actually synthesizing it onto the board. There’s also a part where you need to link an Altera library to your project in order to use the memory VHDL file. This step wasn’t exactly intuitive. Work with a partner. This project is a lot of work. It helps a great deal if you have two or three people working on it. The last thing is getting started early. Debugging this project will take longer than you could possibly imagine. If you encounter problems, it’s much easier to get the TA’s help if it’s a few days before the due date as opposed to the night before.