**Project Feedback**

**by Amol Joshi and Perik Patva**

**Dynamic opcode, single cycle datapath**

a.) What did you learn from this project?

Lectures by Dr. Agrawal gave us knowledge and insight that is needed to build a CPU. But the actual process involves a lot of complications and details. To start with, we got to learn and understand the development process of the ISA- instruction set architecture. With a limit of 16 bits and 16 instructions, much thought was needed to be given to come up with an idea for the opcode format. During this process, we got a chance to learn and try an entirely new approach of opcode design and formation. In our single cycle architecture, we have used a dynamic style of instruction set- which means that the opcode length is not constant but varies as per different instruction. This approach allowed us to access multiple instructions using less number of bits. The other important thing we learnt and was rather useful was VHDL. With no prior experience, the initial project parts took much time, but if you work in groups it shouldn’t be a problem. Our concepts on single cycle datapath became very clear along with realizing the loopholes and issues. Finally, we got to work a bit on the hardware side which was fun.

b.) What would you do differently next time?

As you would read in other feedbacks, we would certainly want to start working on our projects as scheduled. Also, since we took a very different approach this time, we would certainly try to modify it and try to make it better. The few loopholes that we have right now, we would focus on them and try to overcome since they significantly affect the overall performance. Other than that, we would like to try more complex instructions for simulation purpose and try to improve our architecture accordingly. We would certainly like to try new architecture, pipelining in particular since it pretty complex. Using dynamic RISC type ISA on a pipelined architecture might give a very fruitful result.

c.) What is your advice to someone who is going to work on a similar project?

First common advice would be to be on schedule. He would extend the deadlines if needed, but that would spoil the last few parts of the projects – which for graduate students is the demonstration of the hardware. Another important thing to remember is that the compilation of individual components does not necessarily mean those components would function error free when combined together. In case of dynamic opcode single cycle architecture, it will be important and time consuming to develop a VHDL code for the control unit. Also, keep in mind, as you progress with your project, you may find various faults and loopholes in the previous parts. It is very common so don’t worry about it and just keep improving your design in flow with the project. We had to change our datapath multiple times and it turned out to be pretty unconventional, so don’t worry if you come up with something different. Our architecture allows us to use multiple types of single instructions such as – jump, branch… etc. Thus, the control unit could be a little complex, but provides a lot of flexibility. Keep in mind to stay up to date with the deadlines so that you can finish the last part, and feel free to solve your doubts with your teaching assistance, he surely could be of help. Good luck!