ELEC 6200

Final Project – Part 5

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1. While doing this project I realized the internal working of the microprocessors. The complexities that go into designing the processor. This project taught me how to extract the maximum from a processor. From this project I gained many skills like programming in VHDL and also the experience of working with FPGA board. The opportunity to apply the theory learnt in class to design a working processor was very interesting for me. Having designed a multi cycle data path I did not have to face the timing problems of a single cycle data path or the hazard of the pipelining data path. I did have some trouble trying to run the processor on 27MHz clock. I was unable to find why the processor worked on 50MHz clock but not on a 27MHz clock. Theoretically it should not be a problem but practically it did not work.

1. If I could do it over again I would like to try the pipelining data path with all the hazard detection components in it. Being a controls student I would like to try different types of control like micro programmed controller. I would also like to investigate a intelligent controller, that could altogether remove the branch penalties and can handle the hazards in a better way.
2. For someone who is going to do a similar project my advice to you is to simulate every part in modelsim thoroughly so that you do not have any problem while running it on the FPGA board. Debugging in the component stage is much easier than when you have it loaded on the FPGA. If there is a problem while the final execution check the timing of each component. I would also suggest that you try both the clocks on the board, as this caused me some head ache.