Final report on CPU Design Project

1. This project helped us in learning the fundamental steps in designing and implementing a processor. The simulation part of the project using the software tools Modelsim and Quartus II helped us in understanding the interface between the software and hardware tools. In the final step of the project we learned how to simulate our processor on the Altera FPGA board and how to use the In-System memory tools to run our test program straight from the Quartus software.
2. Given a chance to redo the project we will try to implement pipelining as it is an efficient technique. Having the experience we would be more cautious in writing the VHDL code and simulation, test and debugging part. Reducing the critical path delays as much as possible also the complexity of the code to understand would be under consideration.
3. We would recommend students for having a clear insight of functioning of the project before practically implementing it. Understanding the datapath clearly will help in performing the project smoothly. Most important advice is to start the project immediately and verify the simulation of each and every component used in the datapath and also control signals used. By this debugging process while dumping becomes much easier, this is to be started at least one week ahead of the final day. Never hesitate to take help from TA which is always a best option when you’re stuck.

ALL THE BEST !!!!