ELEC 5200-001/6200-001 (Fall 2011)

Homework 4 Problems

Assigned 10/03/11, due 10/10/11

**Problem 1.** Develop a VHDL model for a 4-bit counter with the following specifications:

1. Asynchronous active low Reset signal which sets output of the counter to 0
2. Synchronous active high Enable signal
3. The counter adds 1 on every clock pulse when Enable is active and Reset is inactive

**Problem 2.** Develop a VHDL model for an 8-bit comparator which compares two 8-bit input signals (din1 and din2) with the following specifications:

1. The comparator has three 1-bit outputs: C2, C1 and C0
2. If din1 is less than din2, C2 would be assigned to 1; both C1 and C0 would be assigned to logic 0
3. If din1 is equal to din2, C1 would be assigned to 1; both C2 and C0 would be assigned to 0
4. If din1 is larger than din2, C0 would be assigned to 1; both C2 and C1 would be assigned to 0

**Problem 3.** Develop a VHDL model for a decoder with the following specifications:

1. The decoder has a 2-bit input signal (din) as well as a 4-bit output (dout)
2. If din has a value of 00, dout would be assigned to 0001
3. If din has a value of 01, dout would be assigned to 0010
4. If din has a value of 10, dout would be assigned to 0100
5. If din has a value of 11, dout would be assigned to 1000

**Note**: for problem 1 through 3, please verify the logic function of your VHDL model via ModelSim simulations, write a brief summary about your verification process and submit a hard copy of your VHDL models.