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ELEC 5200

Part 5 Report

While working on this project, I learned many things. The first and foremost was how much thought and consideration must be taken into each aspect of a project of this scope. This was first shown in the designing of the instruction set. Trying to fit all of the functionality into 16 bit words proven to be a difficult task, and every assumption made in this step shaped everything else that was done after it. I learned this because I made a few mistakes in it and essentially started over mid way through the project. I have learned what must be taken into account in the design because of this. From the number of instructions to the addressing of registers and memory, everything must the thought out in advance.

 Having realized this late in the project, if I would look ahead to what hardware limitations my choices in the number of instructions and registers will make. I would also have split up the stages of my pipeline into separate vhdl files so that I could have tested them easier. I would have also started programming hardware units into the hardware so that I could verify functionality before putting them all together. I would have also spend even more time than I had on this attempt. I averaged 10 hours a week on the design and I would now try to do even more.

 If I were to give any advise to future students, it would be to learn the Altera IDE very early in the class. I spent a lot of time attempting to do the same things I had learned in Xilinx IDE, which cost me a lot of time. I would also have read more into how model sim functioned and spent a lot of time running simulations. Finally I would have simulated individual parts into hardware so that I could verify functionality as nothing I synthesized would function once I built the entire processor.